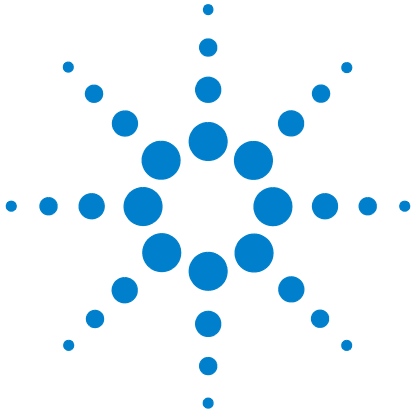

Agilent DigRFv4 Protocol Analyzer

User's Guide

Agilent Technologies

Notices

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Installation Guides

You can find the installation guides for different components of the product on the product CD. Agilent recommends you to do not switch on the instrument before you have understood all the applicable installation instructions and have met all the installation prerequisites.

Where to find more information

You can find more information about DigRF v4 from the following link:

http://www.agilent.com/find/DigRFv4

You can also look for search a local contact for assistance on the following link:

http://www.agilent.com/find/assist

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Indicates warning or caution. If you see this symbol on a product, you must refer to the manuals for specific Warning or Caution information to avoid personal injury or damage to the product.

Frame or chassis ground terminal. Typically connects to the equipment's metal frame.

Indicates hazardous voltages and potential for electrical shock.

Indicates that antistatic precautions should be taken.

Indicates hot surface. Please do not touch.

Indicates laser radiation turned on.

CSA is the Canadian certification mark to demonstrate compliance with the Safety requirements.

CE compliance marking to the EU Safety and EMC Directives.

ISM GRP-1A classification according to the international EMC standard.

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Safety Summary

General Safety Precautions

The following general safety precautions must be observed during all phases of operation of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument.

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Before operation, review the instrument and manual for safety markings and instructions. You must follow these to ensure safe operation and to maintain the instrument in safe condition.

General

This product is a Safety Class 1 instrument (provided with a protective earth terminal). The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

All Light Emitting Diodes (LEDs) used in this product are Class 1 LEDs as per IEC 60825-1.

Environment Conditions

This instrument is intended for indoor use in an installation category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 95% and at altitudes of up to 2000 meters.

Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

Before Applying Power

Verify that all safety precautions are taken. The power cable inlet of the instrument serves as a device to disconnect from the mains in case of hazard. The instrument must be positioned so that the operator can easily access the power cable inlet. When the instrument is rack mounted the rack must be provided with an easily accessible mains switch.

Ground the Instrument

To minimize shock hazard, the instrument chassis and cover must be connected to an electrical protective earth ground. The instrument must be connected to the ac power mains through a grounded power cable, with the ground wire firmly connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective (grounding) conductor or disconnection of the protective earth terminal will cause a potential shock hazard that could result in personal injury.

Do Not Operate in an Explosive Atmosphere

Do not operate the instrument in the presence of flammable gases or fumes.

Do Not Remove the Instrument Cover

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made only by qualified personnel.

Instruments that appear damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

Environmental Information

This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/ electronic product in domestic household waste.

Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control instrumentation" product.

Do not dispose in domestic household waste.

To return unwanted products, contact your local Agilent office, or see www.agilent.com/environment/product/ for more information.

Printing History

Agilent Technologies, Inc. can issue revisions between the product releases to reflect the latest and correct information in the guide. Agilent Technologies, Inc. also reserves its right to not issue a new edition of the guide for every system release.

Manual Name: Agilent DigRFv4 Protocol Analyzer- User's Guide

The edition number of the guide, publishing time of the guide, and applicable release number of the product are given in the following table.

Edition	Published	Applicable Release
1.1	August, 2011	1.9

Contents

1 Agilent DigRFv4 Protocol Analyzer

This chapter introduces the DigRFv4 Protocol Analyzer. It provides an overview of how you can use it for capturing DigRF data and analyzing this data to test and debug a BBIC and RFIC.

Introduction to Agilent DigRFv4 Protocol Analyzer

The Agilent N5343A DigRF Exerciser module and N5344A DigRF Analyzer module provide capabilities to capture the DigRF data either from Tx or Rx line or simultaneously from both the lines over a DigRF link. These hardware modules are a part of the Agilent RDX Test Platform for DigRFv4 solution and are installed in the N5302A/N5304A chassis. To configure and use the capture capabilities of these hardware modules, you create a logical module for DigRF Protocol analysis in the Agilent Logic Analyzer GUI. This GUI also provides a variety of DigRF analysis tools to perform digital data analysis on the captured data or pass this data to Agilent's RF analysis tools for further RF analysis.

The Agilent Logic Analyzer software is installed when you install the RDX test platform software. In the RDX test platform, Logic Analyzer software is integrated with the DigRF Exerciser and Analyzer modules to provide comprehensive features for the capture, display, extraction, and analysis of the DigRF data.

BBIC and RFIC Stimulation

Besides providing the capture capabilities, the RDX test platform for DigRFv4 also provides stimulus capabilities to emulate a BBIC or an RFIC. Using these stimulus capabilities, you can test the DigRF data exchanged with an RFIC/BBIC over the DigRF TxData and RxData sublinks and detect DigRF protocol violations. The stimulus capabilities are provided by the N5343A DigRF Exerciser module. To configure and use the stimulus capabilities of the DigRF Exerciser module, you use the Agilent Protocol Exerciser for DigRF GUI. The stimulus capabilities are therefore not described in this online help. You can refer to the RDX Test Platform for DigRFv4 online help available with the RDX test platform for DigRF software installation to know about the stimulus capabilities. You can also download the RDX Test Platform for DigRFv4 user guide from www.agilent.com.

Rx and Tx Data Capture and Analysis

This online help focusses on capturing and analyzing the Rx and Tx DigRF data using the N5343A DigRF Exerciser module and N5344A DigRF Analyzer module. Refer to the

topics Capturing and Obtaining the DigRF Data for Analysis and Analyzing the Captured DigRF Data in this online help to know more.

RFIC Transmit and Receive Path Testing

In addition to DigRF protocol level testing and analysis, the RDX test platform also enables you to do RF testing and analysis for an RFIC. To help you perform RF testing for an RFIC, the RDX test platform components interoperate with the Agilent RF stimulus and analysis tools such as Agilent Signal Studio software, Signal Generator, and 89600 VSA analysis software. Refer to the Cross Domain Testing of an RFIC on page 97 to know more.

RDX test platform provides an integrated set of digital and protocol analysis tools interoperating with RF measurement tools for a complete test environment for cross-domain RFIC testing. These tools together help you characterize the digital and wireless behavior of RFIC. The cross domain testing features can also help you rapidly verify and integrate DigRFv3 and DigRFv4 based RFIC and BBIC. Refer to the Testing BBIC and RFIC Integration on page 103 to know more.

Uses

You can use the capture capabilities provided by the N5343A DigRF Exerciser module and N5344A DigRF Analyzer module in multiple ways to suit your testing requirements. Some of the broad uses in the context of the capture and analysis of DigRF data are listed below.

- By using the N5343A DigRF Exerciser module as a data capture tool, you can capture the Rx as well as Tx data between the DigRF Exerciser and DUT over the DigRF link. You can then analyze this captured data using a variety of DigRF Analysis tools to perform digital data analysis.
- By using the N5344A DigRF Analyzer module, you can capture and analyze the data from the Tx and Rx lines between an RFIC and BBIC over the DigRF link. Once the data is captured, you can analyze it using a variety of DigRF Analysis tools to perform digital data analysis or pass it to RF analysis tools for further analysis.

- By using the Exerciser/Analyzer module along with the Agilent RF stimulus and analysis tools, you can characterize the RFIC in digital and RF domains. You can provide RF and DigRF stimulus to test the RFIC over the DigRF and RF interface and then analyze the captured data in both domains.
- With the capabilities to characterize the interactions between the RFIC and BBIC, you can isolate defects and optimize performance. This is helpful in determining the root cause of problems during the integration process specifically when the RFIC and BBIC are developed by different vendors.

Refer to the topic Usage Scenarios on page 19 to understand the overall working and usage of these modules in different possible combinations and configurations for data capture and analysis.

Components

This topic briefly describes the hardware and software components of RDX Test Platform for DigRFv4 that you use to capture and analyze the DigRF data. To get a detailed description of these components and how to set up and install these components, refer to the Hardware Guide and Installation Guide of the RDX Test Platform.

The following are the primary hardware and software components.

- DigRF Exerciser Module (N5343A)
- DigRF Analyzer Module (N5344A)
- Chassis
- Probe
- System Controller
- RDX Test Platform software including the Logic Analyzer Software

These RDX test platform components interoperate with the Agilent RF tools such as VSA and Signal studio to provide RF domain testing features. However, these RF tools are not installed as a part of RDX test platform installation.

The following figure illustrates a sample setup of the RDX Test platform with all the components described later in this topic.

Figure 1 RDX Test Platform Components

Hardware Components

DigRF Exerciser Module (N5343A)

RDX Test platform provides the DigRF Exerciser module that you can use as a DigRF stimulus provider and as a DigRF data capture tool.

As a stimulus provider, it can emulate an RFIC or a BBIC and allows you to send customized stimulus (DigRF control and data frames) to an RFIC or a BBIC over the DigRF link. This aspect of the module is not covered in this online help. You use the Agilent Protocol Exerciser for DigRF GUI to configure and use the stimulus capabilities of the module. You can refer to the online help available with this GUI to know about the stimulus capabilities of the module.

As a capture tool, the module provides the dual capture feature that allows you to capture the DigRF frames simultaneously from both Tx and Rx lines over the DigRF link between Exerciser and RFIC/BBIC.

You can plug the DigRF Exerciser module in either a 2 slot or a 4 slot chassis and then connect it to the DUT (RFIC/BBIC) using the N5443A DUT cable.

You can use the Agilent Logic Analyzer GUI to configure, manage, and use the capture capabilities of DigRF Exerciser module. This GUI is installed when you install the RDX Test platform software on the system controller.

DigRF Analyzer Module (N5344A)

RDX Test platform provides the DigRF Analyzer module to capture Rx and Tx traffic between a BBIC and an RFIC for analysis using the DgRF analysis tools. This module transparently monitors DigRF v3 and v4 bus activity, helping you integrate and troubleshoot RFIC/BBIC across a wide variety of over the air standards. This module along with a probe passively monitors and probes the DigRF link when the RFIC and BBIC are integrated.

You can plug the Analyzer module in either a 2 slot or a 4 slot chassis. You can use the Analyzer module alone or along with the DigRF Exerciser module to capture the data for analysis. If used alone, you need to connect the Analyzer module to the DUT and capture the data using either a N5345A soft touch probe or a flying lead probe. If used with

the Exerciser module, you need not connect it to the DUT as it connects to the Exerciser module to get the captured data for analysis.

The DigRF Analyzer module connects to the Agilent Logic Analyzer software to display the captured data for analysis. You use the Logic Analyzer GUI to configure, control, and use the DigRF Analyzer module to capture DigRF data over the DigRF link.

Refer to the help topics in Capturing and Obtaining the DigRF Data for Analysis to know more about the usage of the Analyzer module.

Chassis

You use the N5302A/N5304A Chassis (2 slot or 4 slot) to plug in the DigRF Exerciser and Analyzer module. The chassis is connected to the system controller using the LAN interface or the USB network adapter. Refer to the Hardware guide and Installation guide of RDX test platform to know more about chassis.

Probe

You can use either N5345A Soft Touch Probe or N5346A Flying Lead Probe to passively probe the DigRF link between the integrated RFIC and BBIC with minimal intrusion.

You use a probe with the DigRF Analyzer module to transparently monitor and capture Tx and Rx data over the DigRF link.

Refer to the Hardware guide for RDX test platform to know more about probes.

System Controller

A system controller hosts the software components of the RDX test platform. For instance, it hosts the Protocol Exerciser for DigRF GUI, DigRF Test Wizard, and Logic Analyzer GUI.

The system controller is connected to the chassis which has the DigRF Exerciser / Analyzer modules plugged in. To configure, control, and use the DigRF Exerciser or Analyzer modules, you need to create a session between the system controller and the module using the appropriate RDX test platform GUI hosted on the system controller.

Software Components

RDX Test Platform Software including Logic Analyzer Software

The RDX Test Platform software provides various GUIs to configure, control, and use the DigRF Exerciser and Analyzer modules. The following table describes the purpose of some of the frequently used GUIs of the platform.

GUI	Purpose
Agilent Logic Analyzer GUI	Allows you to configure and use the capture capabilities of DigRF Exerciser and DigRF Analyzer modules. The Agilent Logic Analyzer software is installed when you install the RDX test platform software. In the RDX test platform, Logic Analyzer software is integrated with the DigRF Exerciser and Analyzer modules to provide comprehensive features for the capture, display, extraction, and analysis of the DigRF data.
DigRF Analysis tools and utilities	Agilent Logic Analyzer software provides a number of DigRF Analysis tools and utilities such as: • **Packet Decoder** to decode the DigRF packets captured using the DigRF Exerciser/Analyzer modules. • **Packet Viewer** to view the decoded packets in the Logic Analyzer GUI. • **Signal Extractor** to extract digital IQ data from the captured DigRF packets and do signal analysis or pass the data to the 89601A VSA software for RF domain analysis. • **Signal Inserter** to generate DigRF frames from the input IQ data to use these frames as stimulus to DUT.

You create a session between the GUIs and the DigRF Exerciser/Analyzer module to configure and start the stimulus / capture flow.

Usage Scenarios

RDX Test platform is a flexible and a scalable test solution providing options to set up, configure, and use its software and hardware components in different combinations to suit your specific test scenario.

This topic describes some usage scenarios of the N4343A and N5444A modules of the RDX test platform specifically for capturing and analyzing DigRF data.

Active DigRF protocol level testing and validating a DUT independently

In active DigRF testing scenarios, DigRF Exerciser emulates the peer device and communicates with the DUT (RFIC/BBIC) as an active DigRF link partner over the DigRF link. You can use either the stimulus or capture or both capabilities of DigRF Exerciser to actively test a DUT. The active testing scenarios are described below.

Providing DigRF Stimulus to an RFIC/BBIC for DigRF testing

You can test an RFIC or a BBIC at the DigRF protocol level by stimulating it using the DigRF Exerciser module. DigRF Exerciser can emulate an RFIC or a BBIC to act as the DigRF link partner and exercise and stimulate the DUT with various customized DigRF control and data frames.

By emulating an RFIC or a BBIC, DigRF Exerciser lets you test the DUT independently for DigRF protocol compliance without the peer device availability or interference.

Capturing Tx and Rx DigRF data for digital analysis

You can use DigRF Exerciser to capture the DigRF frames exchanged over the DigRF link for debug and analysis at the digital level. You can capture DigRF data from the Tx and Rx lines simultaneously.

When you want to capture DigRF data from both Tx and Rx lines simultaneously while providing stimulus, you can use the DigRF Exerciser's dual capture feature. Using this feature, you can capture the traffic flowing both ways, that is from the DUT and to the DUT. For dual capturing, Exerciser performs time-corelated capturing that is, it captures the Rx data in relation to the Tx data.

Logic Analyzer software is integrated with the DigRF Exerciser module to get the captured data from this module and display it for analysis.

The following figure depicts a dual capture usage scenario using the DigRF Exerciser module. In this scenario, both the stimulus and capture capabilities of DigRF Exerciser module have been used.

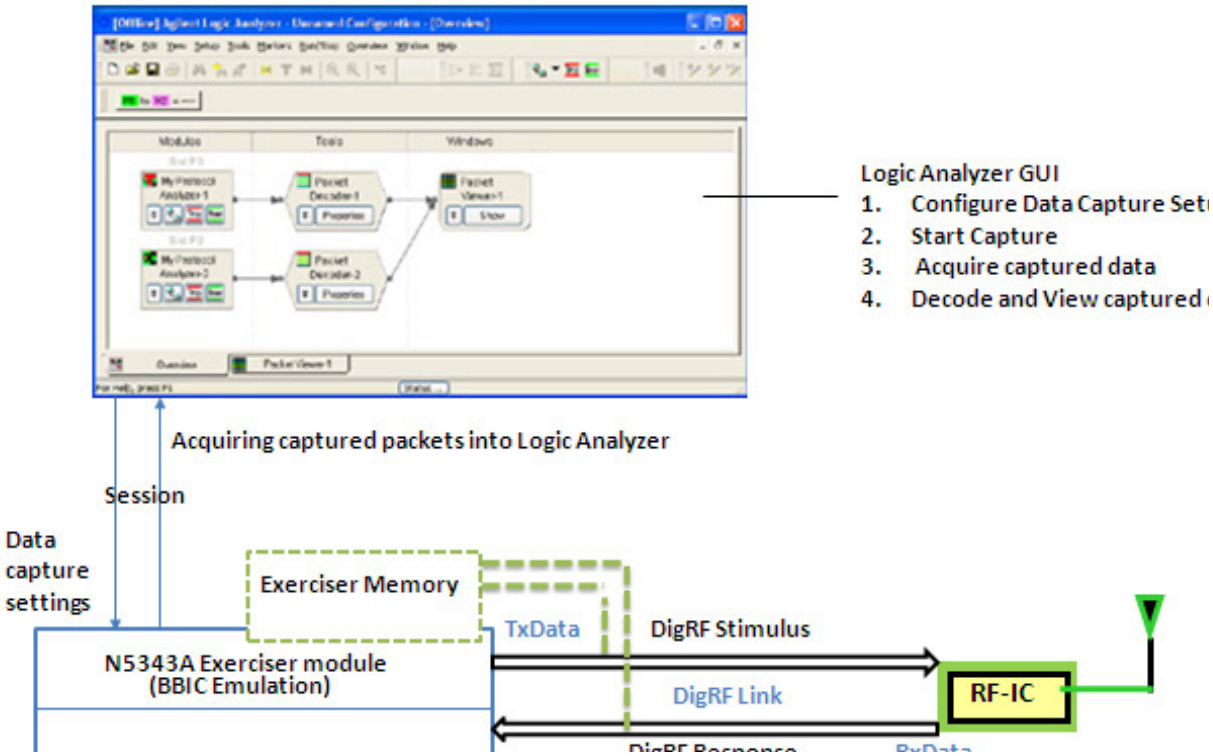


Figure 2 Data capture usage scenario

In the above figure, a connection has been made to a DigRF Exerciser module by creating a session between Logic Analyzer software and DigRF Exerciser module. Using this session, you configure, control, and start the data capture and obtain the captured data from DigRF Exerciser memory and display it in the Logic Analyzer GUI. Once the DigRF packets are available in the Logic Analyzer GUI, you can add DigRF Analysis tools in the Logic Analyzer GUI to analyze the captured data. For instance, Packet Decoder and Packet Viewer are used in the above figure to decode and view the captured DigRF data. You can also use Signal Extractor to extract digital I/Q data from the captured frames and display it with Listing or Waveform windows or send it to the 89601A VSA software for further analysis.

Refer to the topics Configuring a Tx or Rx Data Capture Setup on page 36, Configuring a Dual Capture Setup on page 44, and Obtaining/Acquiring the Captured Data on page 55 to know more about how to use the DigRF Exerciser / Analyzer modules to capture data and how to analyze it using the DigRF Analysis tools.

Passive testing for RFIC and BBIC integration issues

When the RFIC and BBIC are integrated, you can passively probe the DigRF link between these ICs using the DigRF Analyzer module. This enables you to monitor the link transparently with non intrusive probing. The probe captures the data exchanged between an RFIC and a BBIC and provides it to the DigRF Analyzer module. You can view the captured data in Logic Analyzer and then analyze it using various DigRF Analysis tools.

The following figure depicts this usage scenario.

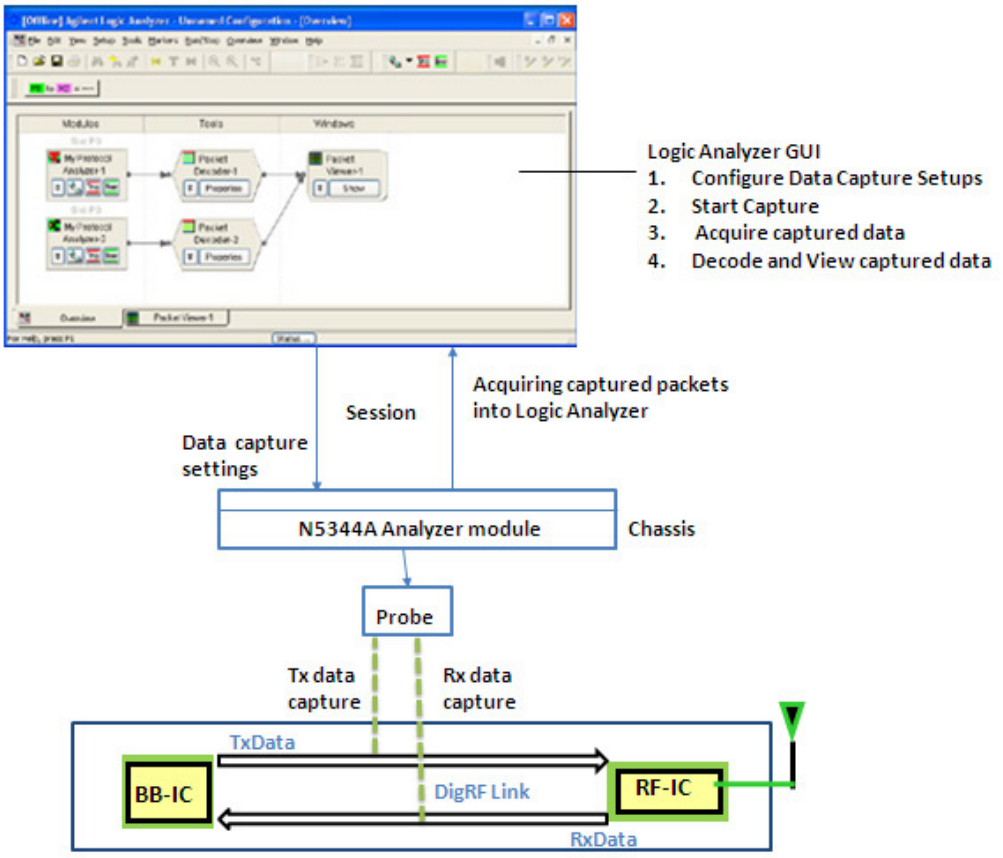


Figure 3 Passive testing

In the above figure, a probe is used on a DigRF link between an RFIC and a BBIC to capture Tx and Rx data. A session is created between the Logic Analyzer software and DigRF Analyzer module to configure the data capture settings and acquire the captured data from the DigRF Analyzer module's memory to Logic Analyzer GUI. The data capture is started from the Logic Analyzer GUI and captured data is decoded, viewed, and analyzed using the DigRF Analysis tools in Logic Analyzer GUI. The captured data helps you analyze whether or not the BBIC and RFIC work together and identify any integration issues between these. Refer to the topic Testing BBIC and RFIC Integration on page 103 to get a detailed description.

RFIC characterization in digital and RF domains

You can do the complete testing of the Transmit and Receive paths of an RFIC in digital and RF domains using the Agilent RF tools in combination with RDX test platform components. Together, these provide digital stimulus and analysis for the digital IQ data and RF stimulus and analysis for the RF antenna side to help you do cross domain testing of an RFIC.

You can validate whether or not the RFIC is able to:

- generate the digital IQ data and packetize it in DigRF frames for transmission over the DigRF link to BBIC.
- receive the DigRF frames from BBIC over the DigRF link, depacketize these into IQ data, and transmit over the air interface.

The following figure depicts the usage of RDX test platform with Agilent RF tools to do RFIC testing in digital and RF domains.

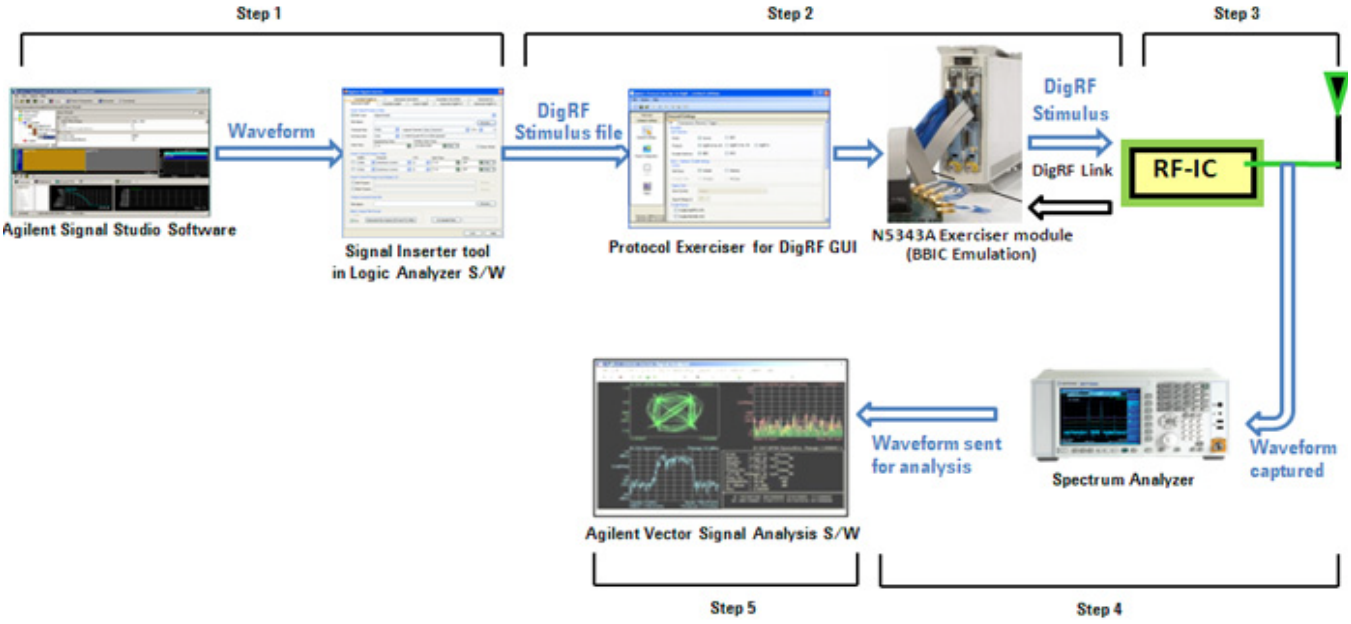


Figure 4 RFIC Testing

In the above figure, the RFIC transmit path (transmitting to air interface) testing is done. Refer to the topic Cross Domain Testing of an RFIC on page 97 to get a detailed description.

2 Testing and Validating an RFIC or a BBIC over the DigRF link

This chapter describes how you can test and validate a BBIC or an RFIC over the DigRF link by using the capture capabilities of the DigRF Exerciser and Analyzer modules.

This chapter also provides some examples of how you can use the captured DigRF data to perform DigRF protocol testing and analysis.

Generating DigRF Stimulus

Overview

To provide DigRF stimulus to an RFIC or a BBIC, you use the stimulus capabilities of the N5343A DigRF Exerciser module. This module provides two GUIs - Protocol Exerciser for DigRF and DigRF Test Wizard to configure and start the stimulus flow. The online help that accompanies each of these GUIs describe the stimulus capabilities in detail.

This online help only covers how to generate a DigRF stimulus file using the Signal Inserter tool that gets installed with the Agilent Logic Analyzer software. You can use this generated stimulus file to send control and data DigRF frames as stimulus from the DigRF Exerciser module to an RFIC/BBIC.

Generating DigRF Stimulus Using the Signal Inserter tool

You can generate DigRF stimulus to stimulate an RFIC or a BBIC from DigRF Exerciser emulating the other link partner by using the following two ways:

- Generating a DigRF stimulus file having a sequence of data ad control frames using the Signal Inserter tool.
- Creating data and control frames using the frame templates available in the Protocol Exerciser for DigRF GUI or the DigRF Test Wizard GUI. You can refer to the online help accompanying each of these GUIs to know more about this method of generating stimulus.

This topic describes how you can generate a DigRF stimulus file using the Signal Inserter tool. This tool converts the raw IQ data and user-defined control information to DigRF compliant data and control frames in a DigRF stimulus file. After generating the DigRF stimulus file, you can import the frames contained in this file into the Frame Configuration page of the Protocol Exerciser for DigRF GUI. These imported frames can then be sent as stimulus to DUT. Refer to the online help available with the Protocol Exerciser for DigRF GUI to know more about importing frames from a stimulus file.

A stimulus file created using Signal Inserter can ease the procedure of setting up or initializing a DUT by sending stimulus in a predefined controlled sequence.

You can insert either the control or data frames or a combination of both control and data frames in a stimulus file generated using Signal Inserter.

The following are the key components in the generation of a DigRF v4 compliant stimulus file using Signal Inserter:

- **Input signal file for generation of data frames** - In Signal Inserter, you can use an IQ data signal file as the input file for the generation of DigRF data frames. Signal Inserter supports various types of file formats for this input signal file. For instance, you can use a signal file generated using Agilent's Signal Studio software as the input file or a two column ASCII decimal file as the input file format.
- **Settings for the generation of DigRF packets from the input signal data** - You specify the DigRF related settings such as Data format or customized IQ data size and number of IQ pairs and the data rate. Based on these settings, Signal Inserter generates DigRF frames from the input signal data.
- **Input file for the generation of control frames** - You specify the ASCII format CSV input files to insert control frames in the Init and Main blocks of DigRF Exerciser while providing stimulus.
- **Output Signal Inserter stimulus file** - You specify the name and location of the output Binary Data file (.bdf) and Licensed Binary Data File (.ldf) that you can use as the DigRF stimulus file. Based on the input signal file and input files for control frames, Signal Inserter generates DigRF data and stores this data in the specified output file. The output files (.bdf and .ldf) are generated along with the TCL script.

To generate a DigRF stimulus file

1 Launch the Signal Inserter tool by clicking Start > Programs > Agilent Logic Analyzer > Signal Inserter option on the Windows task bar.

  The **Agilent Signal Inserter** tool is displayed.

2 There are following tabs to generate DigRF stimulus.

  - Click the **Generate DigRFv3** tab to generate a DigRF V3 complaint stimulus file.
  - Click the **Generate DigRFv4** tab to generate a DigRF V4 complaint stimulus file.

3 Click the **Help** button to get a detailed description of fields in each of these tabs.

4 After specifying the input files, DigRF settings, and output file name and location, click the **Generate the Output LDF and TCL files** button.

Signal Inserter file - Example

The following screen displays the options set in Signal Inserter to generate a DigRFv4 complaint stimulus file containing a sequence of data frames of the LTE R8 Rx format. A Signal Studio file (.wfm) is used as the input signal file. HS Primary 1.x has been selected as the speed mode for the transmission of these data frames as stimulus to BBIC.

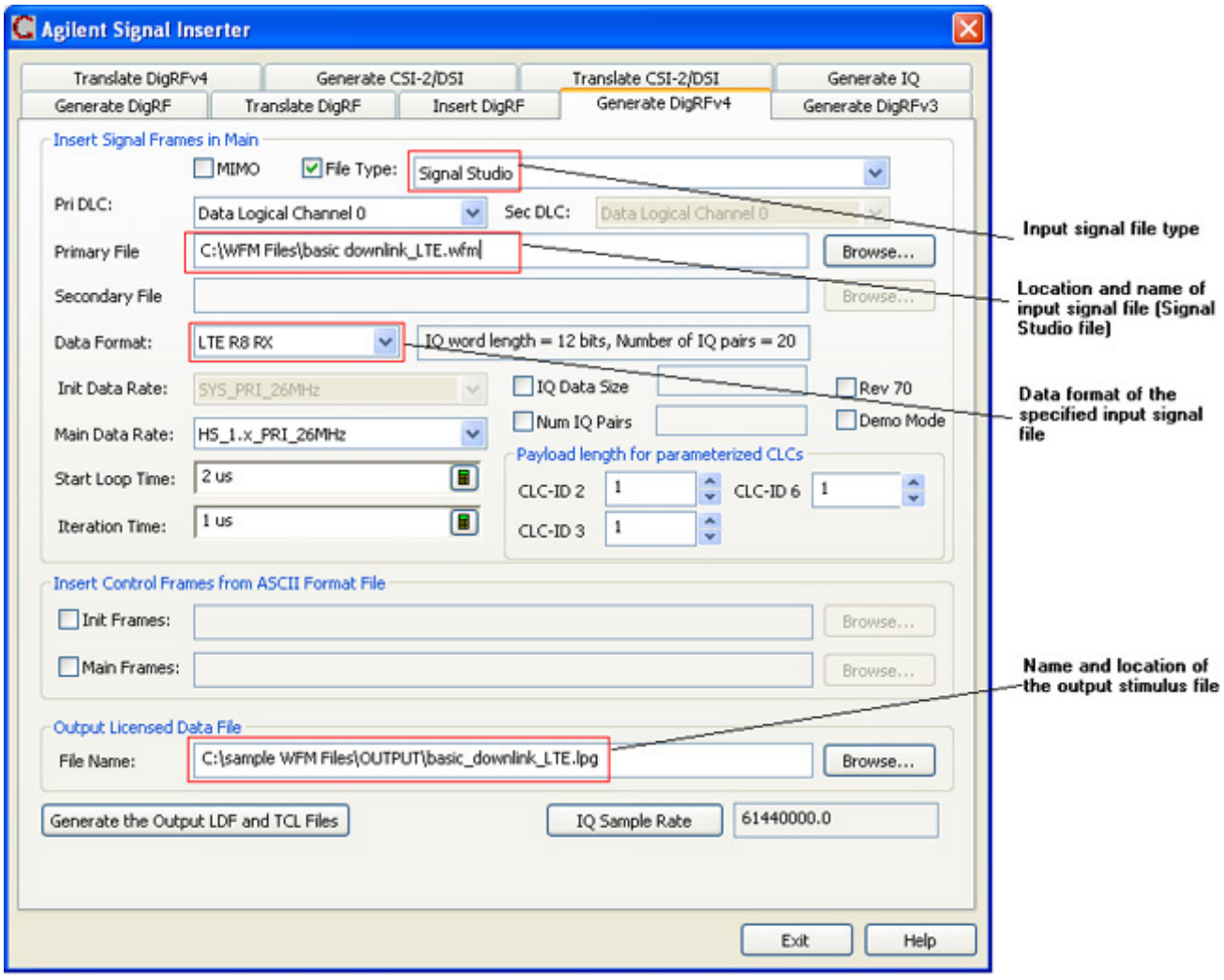


Figure 1 Settings for a DigRFv4 compliant stimulus file

As per the settings displayed above, the following three files are generated at the specified location on clicking the Generate the Output LDF and TCL files button:

- Basic_downlink_LTE.lpg
- Basic_downlink_LTE.ldf
- Basic_downlink_LTE.bdf
- Basic_downlink_LTE.tcl

DigRF frames from the Basic_downlink_LTE.ldf and Basic_downlink_LTE.bdf file can be imported in the Protocol Exerciser for DigRF GUI to send these data frames as stimulus.

Capturing and Obtaining the DigRF Data for Analysis

Overview

The following diagram illustrates the basic sequence of the capture flow using the N5343A Exerciser/N5344A Analyzer modules followed by a brief description of this flow.

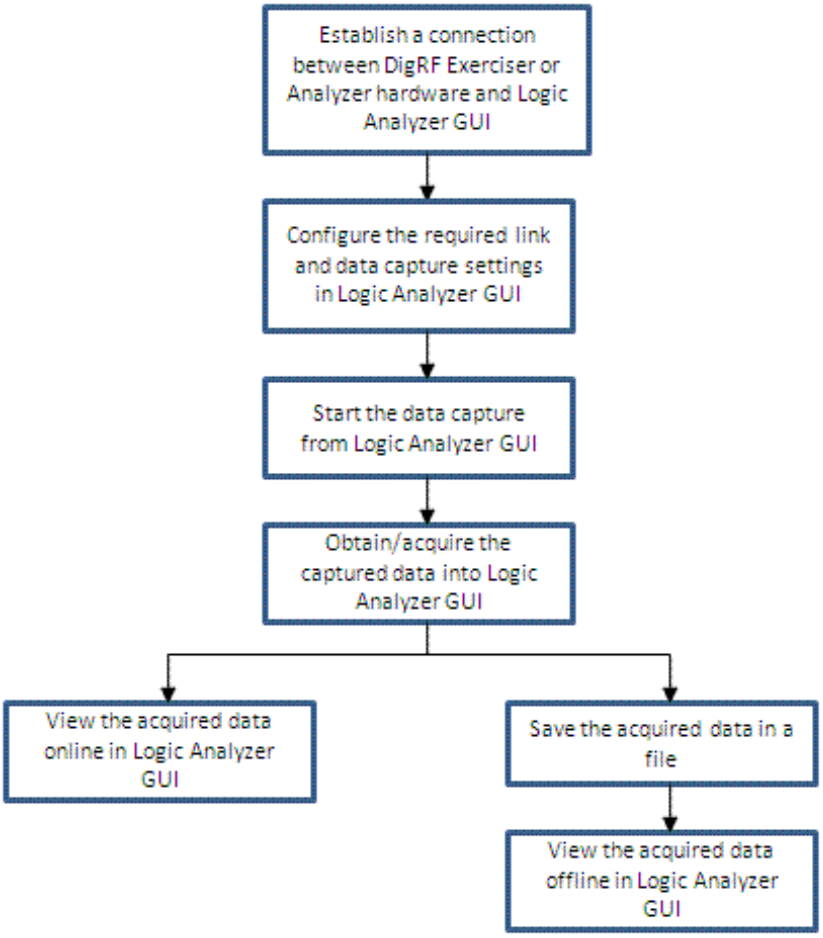


Figure 2 Capture flow

Capturing DigRF data

In RDX Test platform, you can use the following modules to capture DigRF data for validation and analysis:

- **DigRF Exerciser module (N5343A)**: You should use this module when you want to test and analyze an RFIC or a BBIC independent of the other link partner. DigRF Exerciser emulates the other link partner in this case. Using this module, you can capture either the TxData or RxData or the traffic flowing both ways, that is from the DUT to DigRF Exerciser and vice versa.
- **DigRF Analyzer module (N5344A)**: You should use this module when you want to capture the data exchanged between the integrated RFIC and BBIC to analyze and resolve the integration issues. Using this module, you can capture either the TxData or RxData or the traffic flowing both ways between the RFIC and BBIC.

For data capture, a session is needed with the DigRF Exerciser or Analyzer module to establish a connection between the module and the Logic Analyzer GUI. Then, you need to configure the link and data capture settings based on which the data capture is done.

Obtaining DigRF data

After capturing, you need to obtain/acquire the DigRF data captured using either DigRF Exerciser or Analyzer module into the Logic Analyzer GUI for viewing and analyzing it.

Viewing the captured DigRF data

You can use various DigRF Analysis tools to view and analyze the DigRF data obtained in the Logic Analyzer GUI. There are two ways to view the obtained data in Logic Analyzer GUI:

- **Online** - This method requires a connection between the Logic Analyzer GUI and the DigRF Exerciser / Analyzer hardware.
- **Offline** - This method does not require a connection between the Logic Analyzer GUI and DigRF Exerciser/Analyzer hardware used for capturing data. While obtaining the captured data from the module, you can save the data in a file and later view it offline in the Logic Analyzer GUI.

VSA integration capability

You can choose to integrate the run routines of Agilent's 89601A VSA and Agilent Logic Analyzer software so that VSA can draw real-time graphs from the data captured using the DigRF Exerciser/Analyzer module.

The topics that follow describe how to capture the TxData, RxData, or both sides data, how to obtain this data in Logic Analyzer GUI, and how to view it in online and offline modes.

Establishing a Connection with DigRF Exerciser/Analyzer Module

To capture Tx or Rx DigRF data, you first need to establish a connection between the Logic Analyzer GUI and the DigRF Exerciser or Analyzer module that you have decided to use for the data capture. By establishing this connection, you can control, configure, and use the data capture capabilities of the DigRF Exerciser or DigRF Analyzer module through the Logic Analyzer GUI.

You establish this connection by creating a session or using an existing session on the system controller PC that hosts the Logic Analyzer GUI. Before establishing the connection, ensure that the system controller PC is connected to the chassis that has the DigRF Exerciser or Analyzer module hardware.

To establish a connection

1 Launch the Logic Analyzer GUI by clicking **Start > Programs > Agilent Logic Analyzer > Agilent Logic Analyzer** option on the Windows task bar.

   The **Offline Startup Options** dialog box is displayed.

2 Click **Continue Offline** to start the Logic Analyzer application in offline mode, that is, not connected to the Logic Analyzer hardware. To perform DigRF data capture or analysis, you do not need connectivity to the Logic Analyzer hardware.

   The **Agilent Logic Analyzer** GUI is displayed.

3 Click **Setup > Add External Protocol Analyzer....** from the main menu of Logic Analyzer GUI.

   The **External Protocol Analyzer** dialog box is displayed. You use this dialog box to create a session, use an existing session, and setup and control the data capture.

4 Depending on whether you are using DigRF Exerciser or Analyzer module for data capture, select **DigRFv4Exerciser** or **DigRFv4Analyzer** as the session type from the **Select Session Type** listbox.

5 If a session already exists with **DigRFv4Exerciser** or **DigRFv4Analyzer**, use that session by:

   a Clicking **Get Session List** to display a list of available sessions of the selected session type in the open list.

   b From the list of sessions available on the server, selecting a session and then clicking **Connect to a Session**.

Connected appears in the **Connected** column for the selected session which indicates that a connection has been created with DigRF Exerciser/Analyzer module.

6 If a session does not exists, you can create a new session with **DigRFv4Exerciser** or **DigRFv4Analyzer**:

a Click **Create New Session**.

The **Create New Session** dialog box is displayed.

b The module number for the DigRF Exerciser or the Analyzer module connected to the system controller are displayed along with the status of the module. Select the module with which you want to create a session for data capture.

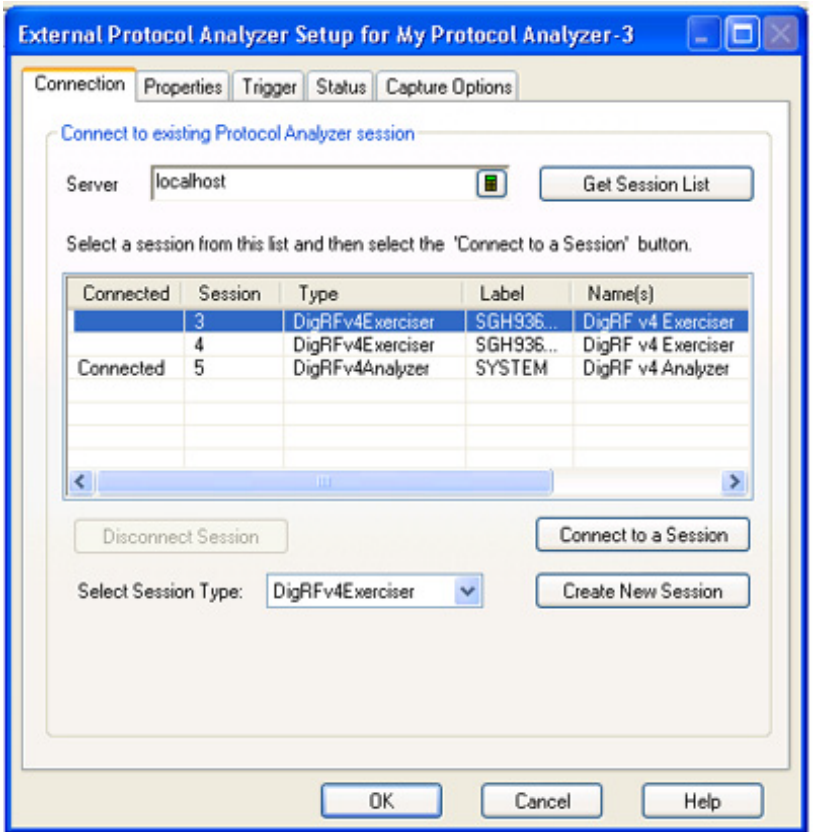
c Click **OK**.

A new session is created with the selected module. The session details are displayed in the Session list.

7 Select this newly created session from the list and click **Connect to a Session**.

Connected appears in the Connected column for the selected session which indicates that a connection has been created with DigRF Exerciser/Analyzer module.

Once a connection is successfully established through a session, the following additional tabs (besides the Connection tab) are added in the External Protocol Analyzer dialog box.



You can then use these additional tabs to configure and control the data capture with the selected DigRF Exerciser or Analyzer module with which the session has been created.

Configuring a Tx or Rx Data Capture Setup

When a session is created between the DigRF Exerciser / Analyzer module and the Logic Analyzer GUI, you can configure the data capture settings for the DigRF Exerciser/ Analyzer module. For instance, you can configure the DigRF link direction for which data capture should be done, a trigger condition that should start the data capture, and the frames that you want the module to capture.

To configure these settings for data capture, you use various tabs in the External Protocol Analyzer Setup dialog box in Logic Analyzer GUI. This is the same dialog box using which you created a connection between the DigRF Exerciser / Analyzer module and the Logic Analyzer GUI. After creating a connection, the relevant tabs are automatically added in this dialog box for configuring the data capture.

This topic describes how to configure the data capture settings to capture data over either a TxData or an RxData sublink using DigRF Exerciser / Analyzer module. To know how to perform dual capture on a DigRF link, refer to the topic Configuring a Dual Capture Setup on page 44.

To configure a Tx or Rx data capture setup, you need to set:

- a connection with DigRF Exerciser/Analyzer module
- link and data capture properties
- trigger condition(s) if you want to start capture on a trigger
- checks to be performed on the frames received in capture memory of DigRF Exerciser/Analyzer

Connection with DigRF Exerciser/Analyzer module

1. In the Logic Analyzer GUI, access the External Protocol Analyzer Setup dialog box for the module that you added with the connection to the DigRF Exerciser or Analyzer hardware. To do this, click the Connection Setup icon displayed in the module that you added for data capture in the Overview tab of the Logic Analyzer GUI. To know how to create a connection, refer to the topic Establishing a Connection with DigRF Exerciser/Analyzer Module on page 33.
2. Ensure that a session is created in the Connection tab with the DigRF Exerciser / Analyzer module.

Set link and data capture properties

1 Click the **Properties** tab in the **External Protocol Analyzer Setup** dialog box.

2 Select the link direction in which you want to do data capture.

If you are using DigRF Exerciser for data capture:

- **Tx** means the data transmitted by DigRF Exerciser will be captured.
- **Rx** means the data received by DigRF Exerciser will be captured.

If you are using DigRF Analyzer for data capture:

- **Tx** means data transmitted on the TxData sublink (BBIC to RFIC) will be captured.
- **Rx** means data transmitted on the RxData sublink (RFIC to BBIC) will be captured.

3 Select the DigRF protocol applicable for the DigRF link on which you want to perform data capture. There are two options, V4 which means DigRFv4 0.60 and V3 which means DigRFv3. If you select the REV 70 checkbox, it means the DigRFV4 0.70 protocol.

4 From the **RX Lanes** group box, select the number of lanes on which data is received in the capture memory of DigRF Exerciser or Analyzer module. For instance, if you are capturing the data transmitted by Exerciser (Tx data), then number of lanes are applicable for the Tx lanes of Exerciser. If you are using DigRF Exerciser to provide stimulus for this data capture, then the number of lanes should not clash with the number of lanes set for the stimulus in the Protocol Exerciser for DigRF GUI. If it clashes, then the data is not captured. By default, the number of lanes match the number of lanes set in the stimulus settings.

5 In the **RX Polarity** group box, set the polarity for the lanes on which data is received in the capture memory of DigRF Exerciser or Analyzer module. If you are using DigRF Exerciser to provide stimulus for this data capture, then the polarity of lanes should not clash with the polarity of lanes set for the stimulus in the Protocol Exerciser for DigRF GUI. If it clashes, then the data is not captured. By default, the polarity of lanes match the polarity set in the stimulus settings.

6 From the **Clock Source** group box, select the source for the reference clock if you are using DigRF Exerciser module for data capture. You can choose from the following options:

- **Internal**: Select if you want to use DigRF Exerciser's internal or onboard oscillator clock as the source.
- **External**: Select if you want to use an external clock source, such as a DUT clock source, for DigRF Exerciser.

7 Currently, only 26 MHZ is supported as the clock speed in a capture setup.

8 From the **Mode** group box, select the speed mode for the data capture. If you are using DigRF Exerciser to provide stimulus for this data capture, then the speed mode should not clash with the speed mode set for the stimulus in the Protocol Exerciser for DigRF GUI. If it clashes, then the data is not captured. This is applicable only for a DigRF v4 link.

9 From the **Rate** group box, select the DigRF interface line rate. This is applicable only for a DigRF v4 link. The effective Tx or Rx link speed is also displayed based on the **Mode** and **Rate** combination selected.

10 In the **Capture Setup** group box, choose which frames you want to store in the capture memory of DigRF Exerciser/Analyzer. You can store:

- either all the frames in the configured link direction.
- only those frames in the configured link direction whose first four bytes match the specified pattern.

11 From the **Maximum Capture memory** percentage slider, select the percentage of the capture memory of DigRF Exerciser module that you want to allocate for the storage of data captured in the configured link direction. This lets you divide the capture memory between Tx and Rx data captured using the DigRF Exerciser module. This step is not applicable if you are using the DigRF Analyzer module for data capture. Unlike the DigRF Exerciser module, the capture memory of DigRF Analyzer module is not divided between the Tx and Rx data capture.

NOTE The DigRF Exerciser and Analyzer modules have 512 MB of capture memory to store the captured data. Out of this 512 MB of memory, the captured data is stored in 380 MB. The rest of memory (approximately 132 MB) is consumed by internal bookkeeping logic. If you are capturing data using the DigRF Exerciser module, you can divide this 380 MB between the Tx and Rx data captured.

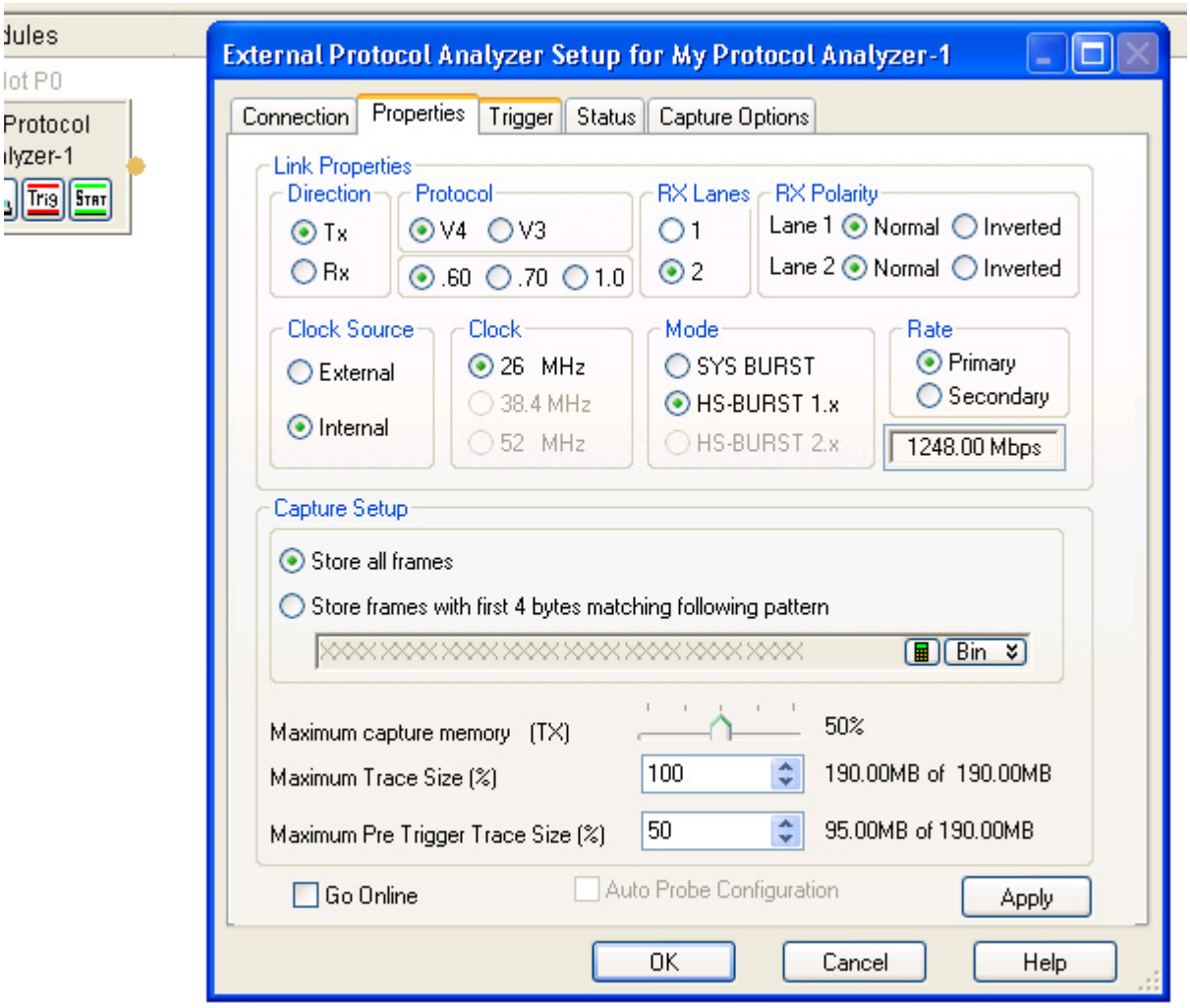
12 In the **Maximum Trace Size (%)** field, specify the percentage of the maximum capture memory of Exerciser/Analyzer module to be used for storing the total (pre and post trigger) capture trace.

13 In the **Maximum Pre trigger trace size (%),** specify the percentage of the maximum trace size to be used for storing the captured data before the capture trigger condition specified in the Trigger tab is met. The remainder of the memory allocated for the maximum trace size is used for storing post trigger data capture.

14 Select the **Go Online** checkbox to ensure that clicking the  **Run** toolbar button starts the data capture as well as uploads the captured data from the memory of DigRF Exerciser/Analyzer into Logic Analyzer GUI for display and analysis. If this checkbox is not selected, then you first need to start the data capture using the **Start** button in the Status tab of this dialog box. Then, you need to click the  **Run** toolbar button to upload the captured data from the memory of DigRF Exerciser/Analyzer into Logic Analyzer GUI. Selecting this checkbox eliminates the need for explicitly clicking the Start button to start the data capture. Refer to the topics Starting the Data Capture on page 52 and Obtaining/Acquiring the Captured Data on page 55 to know more.

15 Select the **Auto Probe Configuration** check box to ensure that the probe used with the DigRF Analyzer module to passively probe the link is automatically configured as per the data capture settings. This option is disabled if you use DigRF Exerciser for data capture.

The module that you added for data capture in the Overview tab of the Logic Analyzer GUI now contains the link and data capture settings. The following screen displays a module that has the settings for capturing the data transmitted from the DigRF Exerciser module.



Set trigger condition(s) to start capture on a trigger

In this tab, you can enable the data capture to start only when a specified trigger condition is met. The data captured when the trigger condition is met is stored in the post trigger capture memory of DigRF Exerciser/Analyzer module. The maximum size of the post trigger capture trace is determined by the capture memory settings that you

configured in the Properties tab. The capture stops automatically when the allocated post trigger capture memory is full.

1 Click the **Trigger** tab in the **External Protocol Analyzer Setup** dialog box.

2 Select the **Enable capture on trigger** checkbox to ensure that the data capture starts only when the trigger condition(s) that you specify in this tab are met.

3 Specify the patterns that serve as the conditions to start data capture. You can specify upto four patterns, each comprising of four bytes with the first byte to match the header and the next three bytes to match the payload of a captured frame. During the data capture flow, the header and payload of the frames in the configured link direction are checked against these patterns. If the first four bytes of a frame (first byte for header and the next three bytes for payload) match with one of these patterns, the trigger condition is met and the data is stored in the post trigger capture memory. You can also use a value of XX in a pattern to indicate that this byte in the pattern can match any value in the corresponding byte in the frame. Also, if you specify a pattern value with less than four bytes, the remaining bytes in the pattern are automatically filled by XX to match any value for these bytes in the frame. For instance, if you specify the pattern as XX55FF55 Hex, then the frames with any value in the header and 55FF55 pattern for the first three bytes of payload will trigger the data capture. To get an example of trigger patterns, refer to the topic Example - DigRF Data Capture on page 68.

4 You can select the **Trigger out** checkbox displayed with each pattern field to send a trigger out pulse when a frame in the configured link direction matches the pattern. The trigger out pulse is sent from the DigRF Exerciser/Analyzer module that you used for data capture to the test equipment connected to its Trigger Out Connector pin.

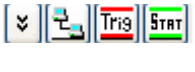
5 Besides specifying patterns as the trigger conditions, you can also specify an external trigger in signal as the trigger condition to start data capture. If you select the **External trigger in** checkbox, the data capture starts when a trigger in signal is received by DigRF Exerciser/Analyzer module on its Trigger in connector pin from another test equipment.

To get an example of trigger conditions set for the data capture, refer to the topic Example - DigRF Data Capture on page 68.

Set checks to be performed on the captured frames

1. Click the **Capture Options** tab in the **External Protocol Analyzer Setup** dialog box.
2. Deselect the checkboxes in the **Receive frame checks** group to enable the frame level checks to be performed on the captured frames. You can deselect the Disable CRI checking checkbox to ensure that the captured frames are checked for the missing or incorrect CRI number. Based on the checks that you select here, the Error counters in the Status tab are updated for the errors encountered in the captured frames.
3. In the **Expected length of DLC frames** group box, set the expected length of the captured data frames. DigRF Exerciser uses this length to check A captured data frame is checked to match the expected length specified for that DLC type. A **Frame with length error** is reported in the Status page if length checking is enabled and a captured data frame crosses the expected length.
4. The **Probe Configuration** group box is enabled if you are using the DigRF Analyzer module for data capture. You can select the type of configurations that you want to use for the probe connected with the DigRF Analyzer module to passively probe the link. If you want to capture high speed DigRFv4 data with lower Sync and Prep values (preferred values - Sync=5 and Prep=4) using the DigRF Analyzer module, then select the V4 Dual Probing configurations for the probe. If dual probing configurations are not used, then in HS-BURST non-continuous mode, DigRF Analyzer can capture data correctly only with higher values of Sync (>10) and Prep (>4).

NOTE You can save the data capture configurations done in the Logic Analyzer GUI in a .ala configuration file. To save the configurations, click File -> Save in the Logic Analyzer GUI.

You can change the link or data capture settings for a module by clicking the  icons displayed on the module.

Once the module is ready with the data capture settings, you can start capturing the data.

Configuring a Dual Capture Setup

This topic describes how you can configure the data capture settings in the Logic Analyzer GUI to capture the bidirectional data (Tx as well as Rx) over a DigRF link. The usage of both DigRF Exerciser and Analyzer module is described to perform dual capture.

Using DigRF Exerciser module

When you perform dual capture using the DigRF Exerciser module, it captures the data that it transmits to the DUT (Tx data) as well as the data that it receives from the DUT (Rx data) over the DigRF link. Both the Tx and Rx data are stored in the Capture memory of the DigRF Exerciser module. You can configure how the total capture memory size of the DigRF Exerciser module should be divided to store the captured Tx and Rx data. The total size of the capture memory of the DigRF Exerciser module is 512 MB. Out of the total 512 MB of memory, the captured data is stored in 380 MB. The rest of memory (approximately 132 MB) is used by internal bookkeeping logic. You can divide this 380 MB of memory between the Tx (data transmitted by DigRF Exerciser) and Rx (data received from DUT) storage.

NOTE To perform dual capture using the DigRF Exerciser module, you should have the required license of the DigRF Exerciser module with the dual capture capabilities. You can add this license using the License Programmer tool.

To configure dual capture setup using the DigRF Exerciser module:

1 Configure the data capture setup for Tx data capture (data transmitted from DigRF Exerciser). To do this:

   a Access the **External Protocol Analyzer Setup** dialog box in the Logic Analyzer GUI.

   b Ensure that a session is created between the DigRF Exerciser module and Logic Analyzer GUI. Refer to the topic Establishing a Connection with DigRF Exerciser/Analyzer Module on page 33 to know more.

   c Follow the steps mentioned in the topic Configuring a Tx or Rx Data Capture Setup on page 36 to create a setup for the Tx data capture. Ensure that:

- the **Link** direction is set to **Tx** in the **Properties** tab to make these settings applicable for Tx data capture, that is capturing the data transmitted by DigRF Exerciser.
- the percentage of total memory that you want to allocate to the Tx data storage is set in the **Maximum Capture Memory (Tx)** field in the **Properties** tab.

2 Configure the data capture setup for Rx data capture (data received by DigRF Exerciser). To do this:

a Access the **External Protocol Analyzer Setup** dialog box in the Logic Analyzer GUI.

b Connect to the DigRF Exerciser module using the same session as used in step 1 (Tx data capture). Refer to the topic Establishing a Connection with DigRF Exerciser/Analyzer Module on page 33 to know more.

c Follow the steps mentioned in the topic Configuring a Tx or Rx Data Capture Setup on page 36 to create a setup for the Rx data capture. Ensure that:

- the **Link** direction is set to **Rx** in the **Properties** tab to make these settings applicable for Rx data capture, that is capturing the data received by DigRF Exerciser.
- the percentage of total memory that you want to allocate to the Rx data storage is automatically set in the **Maximum Capture Memory (Rx)** field in the Properties tab. This setting is calculated based on the memory that you allocated for the Tx data storage in Step 1.

The following screens display a Tx (data transmitted by DigRF Exerciser) and then an Rx (data received by DigRF Exerciser) data capture module.

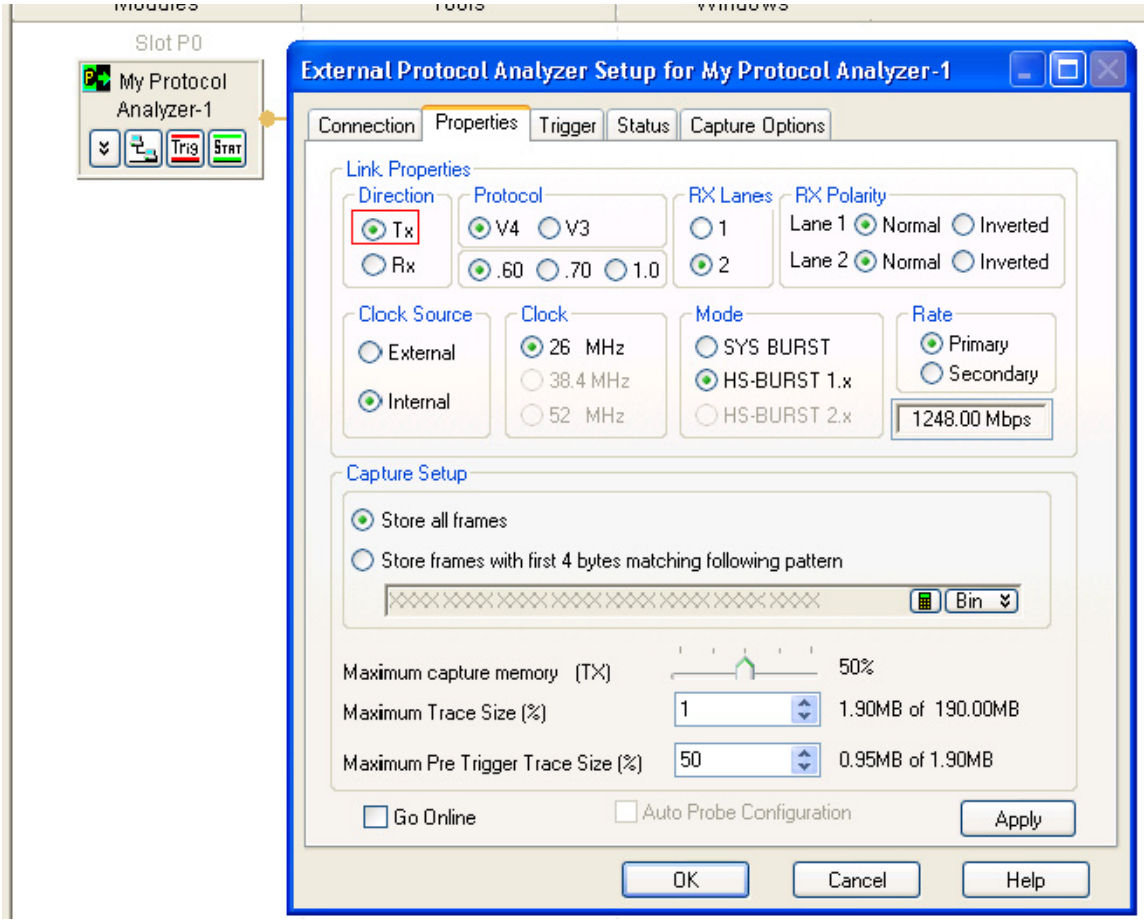


Figure 3 Tx data capture module

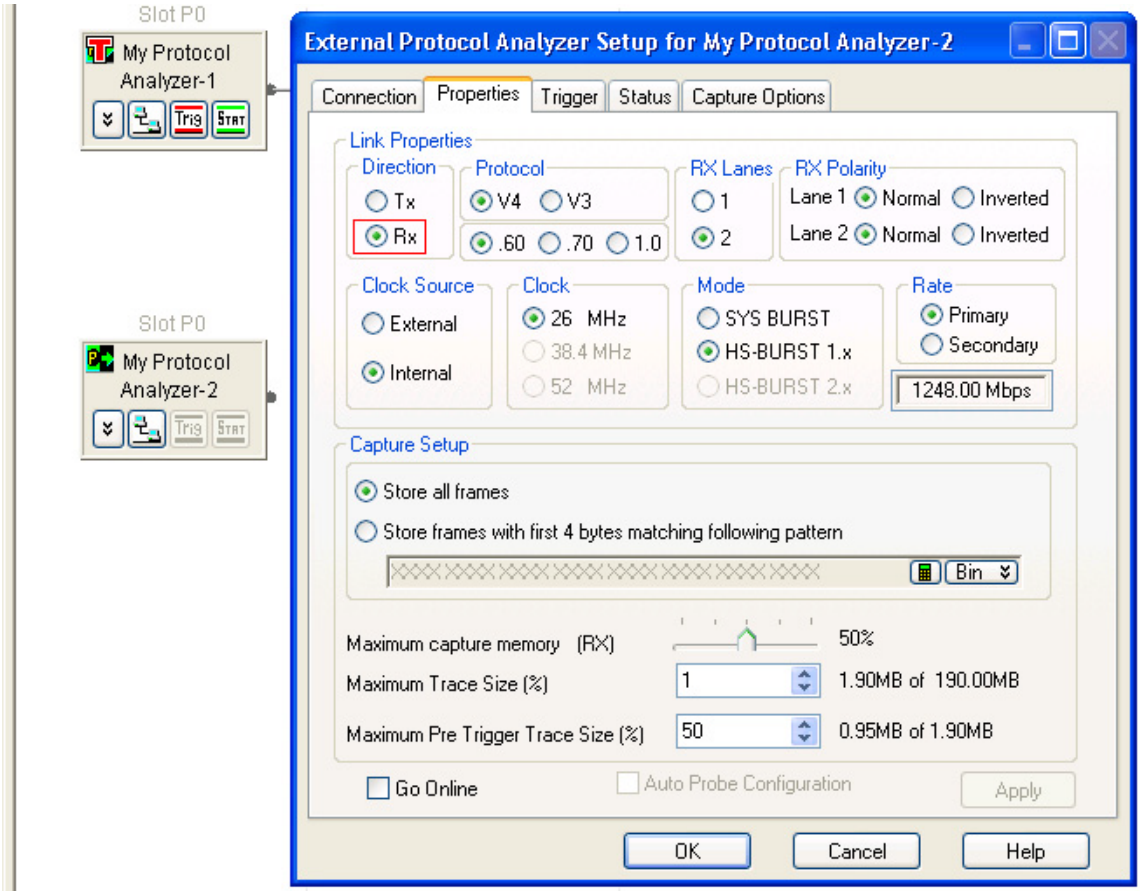
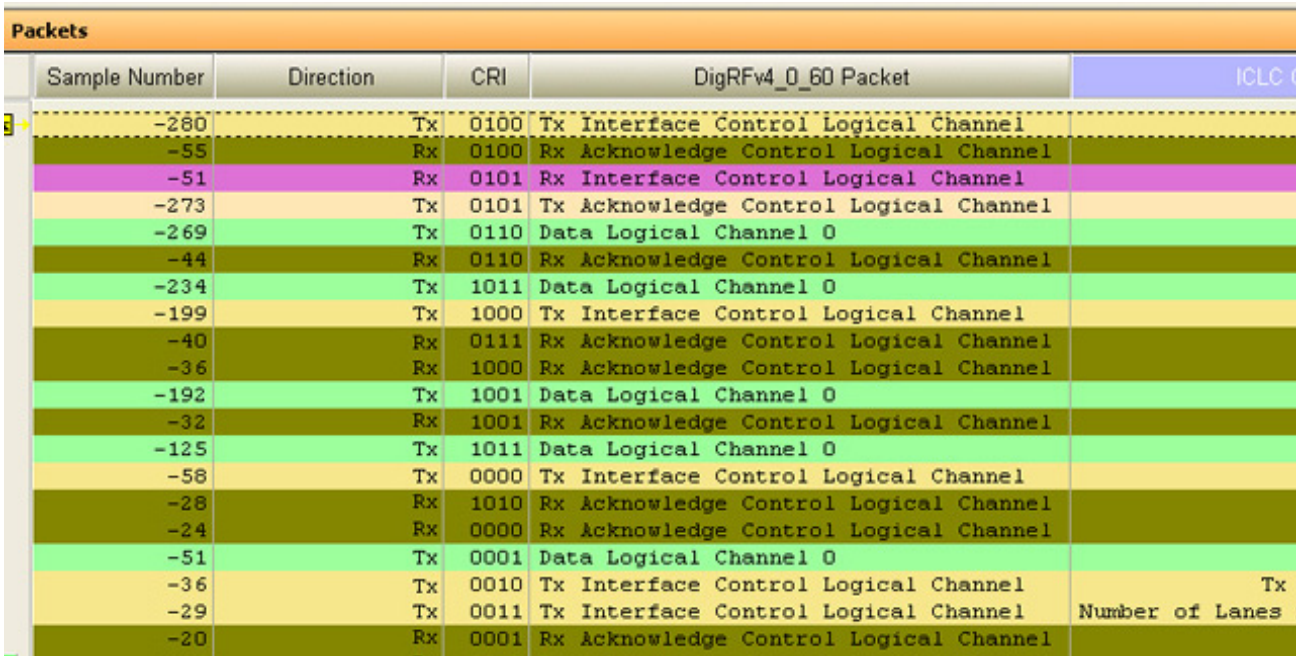


Figure 4 Rx data capture module

Once the data capture module setups are added in Logic Analyzer, you can add the Packet Decoder and Packet Viewer tools to complete the configuration of data capture.

When you start dual capture as per the configured settings, DigRF Exerciser captures the Rx data in relation to the Tx data, that is, it captures the stimulus transmission and the response to the transmission. The following screen displays a sample output of the dual data capture in the Logic Analyzer GUI. To get a detailed example of how to view dual capture data, refer to the topic Viewing the Captured DigRF Data Online on page 58.



Packets

Sample Number	Direction	CRI	DigRFv4_0_60 Packet	ICLC
-280	Tx	0100	Tx Interface Control Logical Channel	
-55	Rx	0100	Rx Acknowledge Control Logical Channel	
-51	Rx	0101	Rx Interface Control Logical Channel	
-273	Tx	0101	Tx Acknowledge Control Logical Channel	
-269	Tx	0110	Data Logical Channel 0	
-44	Rx	0110	Rx Acknowledge Control Logical Channel	
-234	Tx	1011	Data Logical Channel 0	
-199	Tx	1000	Tx Interface Control Logical Channel	
-40	Rx	0111	Rx Acknowledge Control Logical Channel	
-36	Rx	1000	Rx Acknowledge Control Logical Channel	
-192	Tx	1001	Data Logical Channel 0	
-32	Rx	1001	Rx Acknowledge Control Logical Channel	
-125	Tx	1011	Data Logical Channel 0	
-58	Tx	0000	Tx Interface Control Logical Channel	
-28	Rx	1010	Rx Acknowledge Control Logical Channel	
-24	Rx	0000	Rx Acknowledge Control Logical Channel	
-51	Tx	0001	Data Logical Channel 0	
-36	Tx	0010	Tx Interface Control Logical Channel	Tx
-29	Tx	0011	Tx Interface Control Logical Channel	Number of Lanes
-20	Rx	0001	Rx Acknowledge Control Logical Channel	

Figure 5 Dual data capture results

NOTE

To get co-related data from the dual capture setup, ensure that you use the same Packet Viewer window in Logic Analyzer GUI to view the packets captured in Tx as well as the Rx direction. Refer to the topic Viewing the Captured DigRF Data Online on page 58 to know how you can view the bidirectional data captured over a DigRF link.

Using DigRF Analyzer module

You can perform dual capture using the DigRF Analyzer module by monitoring a DigRF link between two DUTs (BBIC and RFIC) and capturing the DigRF data flowing both ways with the help of a flying lead or a midbus probe.

To accomplish dual capture, you need to configure two data capture setups in Logic Analyzer GUI, one for Tx data capture and another for Rx data capture. Here, Tx data capture means capturing data on the TxData sublink that is, BBIC to RFIC. Rx data capture means capturing data on the RxData sublink, that is, from RFIC to BBIC.

Unlike the DigRF Exerciser module, you do not divide the capture memory (380 MB) of DigRF Analyzer into Tx and Rx capture memory.

Once the data capture module setups are added in Logic Analyzer, you can add the Packet Decoder and Packet Viewer tools to complete the configuration of data capture.

NOTE

To get co-related data from the dual capture setup, ensure that you use the same Packet Viewer window in Logic Analyzer GUI to view the packets captured in Tx as well as the Rx direction. Refer to the topic Viewing the Captured DigRF Data Online on page 58 to know how you can view the bidirectional data captured over a DigRF link.

Configuring Data Capture with VSA Integration

This topic describes how you can configure the data capture setup to ensure that the captured data is simultaneously sent from Logic Analyzer to the VSA GUI for further RF analysis. The VSA integration with the data capture enables VSA to generate real time graphs from the captured data received from the Logic Analyzer GUI. This topic describes the configurations that you need to perform on the Logic Analyzer GUI and the VSA GUI to enable integration of VSA while data capture for online analysis of the captured data.

When integrated with data capture, VSA runs to the end of the current Logic Analyzer data capture buffer and instructs or triggers the Logic Analyzer to run again for recapture.

Configuring Logic Analyzer GUI for online analysis using VSA

1. Configure the Tx or Rx data capture setup as stated in the topic Configuring a Tx or Rx Data Capture Setup on page 36. In this capture setup configuration, select the Go online checkbox to ensure that you do not have to manually start and stop data captures in the Logic Analyzer GUI when VSA triggers the Logic Analyzer GUI for recapture.
2. Ensure that the post trigger capture memory of the DigRF Exerciser/Analyzer module is set to 100%. This is necessary so that pre trigger memory is not utilized at all and all the captured data gets filled in the post trigger memory. Refer to the topic Configuring a Tx or Rx Data Capture Setup on page 36 to know how to set this memory.
3. Ensure that the data capture on trigger is enabled with all XX masking as the trigger pattern. This step ensures that the trigger condition is met immediately when the data capture starts and the post trigger memory starts filling. When the VSA trigger type is free-run, it ignores any trigger setup on the Logic Analyzer. VSA then processes the input data as quickly as possible, without waiting for any kind of triggering signal.

Configuring the VSA GUI for online analysis of captured data

1. Start the VSA GUI.
2. Link the VSA GUI to the Logic Analyzer application.
   a. VSA gets the Logic Analyzer address using the 89600 IO Connections software utility. The 89600 IO

Connections software utility is installed with the VSA software and is located at **Start** > (All) **Programs** > **Agilent 89600 VSA** > **Logic Analyzer** > **IO Connections**. If the Logic Analyzer application resides on the same PC as the VSA, then use the name "localhost."

b In the **VSA** GUI, click **Utilities** > **Hardware** > **ADC 1**. Clear **Simulate Hardware** if currently selected and select **Agilent VSA Logic Analyzer Input**. VSA will then link to the Logic Analyzer application.

To get detailed information on configurations in the VSA GUI, refer to the VSA online help.

You also have the option to analyze the captured data in VSA in offline mode, that is no connection is needed with the DigRF Exerciser/Analyzer for analysis. Refer to the topic, Analyzing Captured Data using VSA on page 93 to know more.

Starting the Data Capture

After you have added the required modules with the data capture settings in the Overview tab of the Logic Analyzer GUI, you can start the data capture. On starting the data capture, the hardware (DigRF Exerciser or Analyzer module) that you have selected for data capture, starts capturing the data as per your configured settings. This captured data is stored in the memory of the DigRF Exerciser / Analyzer module as per the maximum capture memory that you specified in the data capture setup. The statistics for data capture are updated simultaneously in the Logic Analyzer GUI to help you ascertain whether or not the frames are getting captured.

NOTE If you are using both the stimulus and capture capabilities of DigRF Exerciser, then ensure that you start the data capture in Logic Analyzer GUI before starting the stimulus in the Protocol Exerciser for DigRF GUI. If this sequence is not followed, the number of frames captured is displayed as 0 in Logic Analyzer GUI.

To start the data capture:

If the Go Online checkbox is not selected in the Properties tab of the External Protocol Analyzer Setup dialog box:

1 In the Logic Analyzer GUI, access the External Protocol Analyzer Setup dialog box for the module that you added with the required data capture settings. To do this, click the  **Status** icon displayed in the module in the Overview tab of the Logic Analyzer GUI.

   The **Status** tab of the External Protocol Analyzer Setup dialog box is displayed.

2 Click the **Start** button in the **Status** tab.

On starting the data capture, the DigRF Exerciser or Analyzer module with which the session is created starts capturing data in the configured link direction (Tx or Rx). The Capture State is displayed as **Running** in the Status tab. The Statistics and error counters for the data capture are simultaneously updated during the capture. However, the total number of frames captured is updated when the data capture stops automatically or you stop it manually.

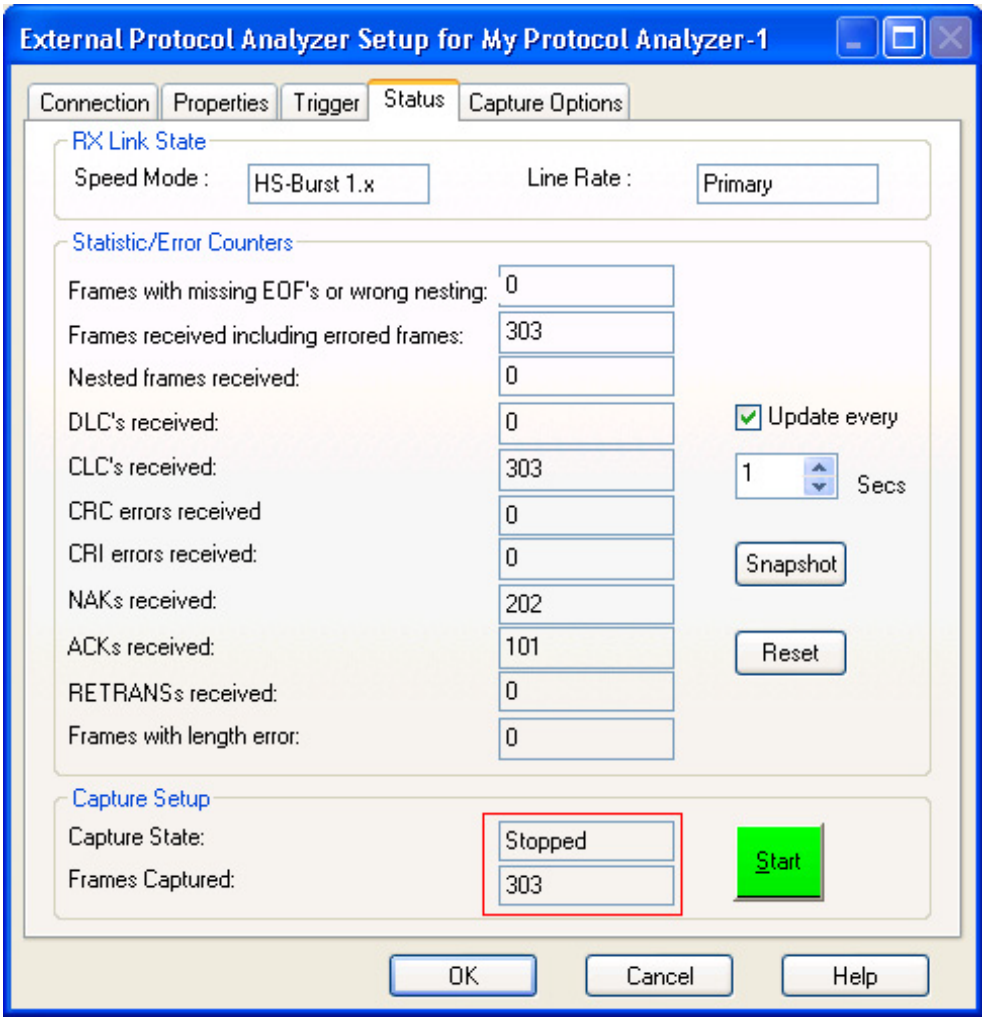


Figure 6 Data capture status

The capture stops:

- automatically when the capture memory of the module that you specified to store the captured data is full.
- if you manually stop the capture by clicking **Stop** in the Status tab of the External Protocol Analyzer Setup dialog box for the module.

NOTE Once the data capture has stopped, you need to obtain/acquire the captured data from the DigRF Exerciser/Analyzer module's memory into the Logic Analyzer GUI by clicking the toolbar button. Once the captured data is obtained in the Logic Analyzer GUI, you can decode the packets and view it using Packet Viewer.

If the Go Online checkbox is selected in the Properties tab of the External Protocol Analyzer Setup dialog box:

1 Click the **Run** toolbar button in Logic Analyzer GUI. Clicking this button starts the data capture as well as uploads the captured data into the Logic Analyzer GUI for display and analysis. In this case, you need not start the data capture using the **Start** button in the **Status** tab of the External Protocol Analyzer Setup dialog box.

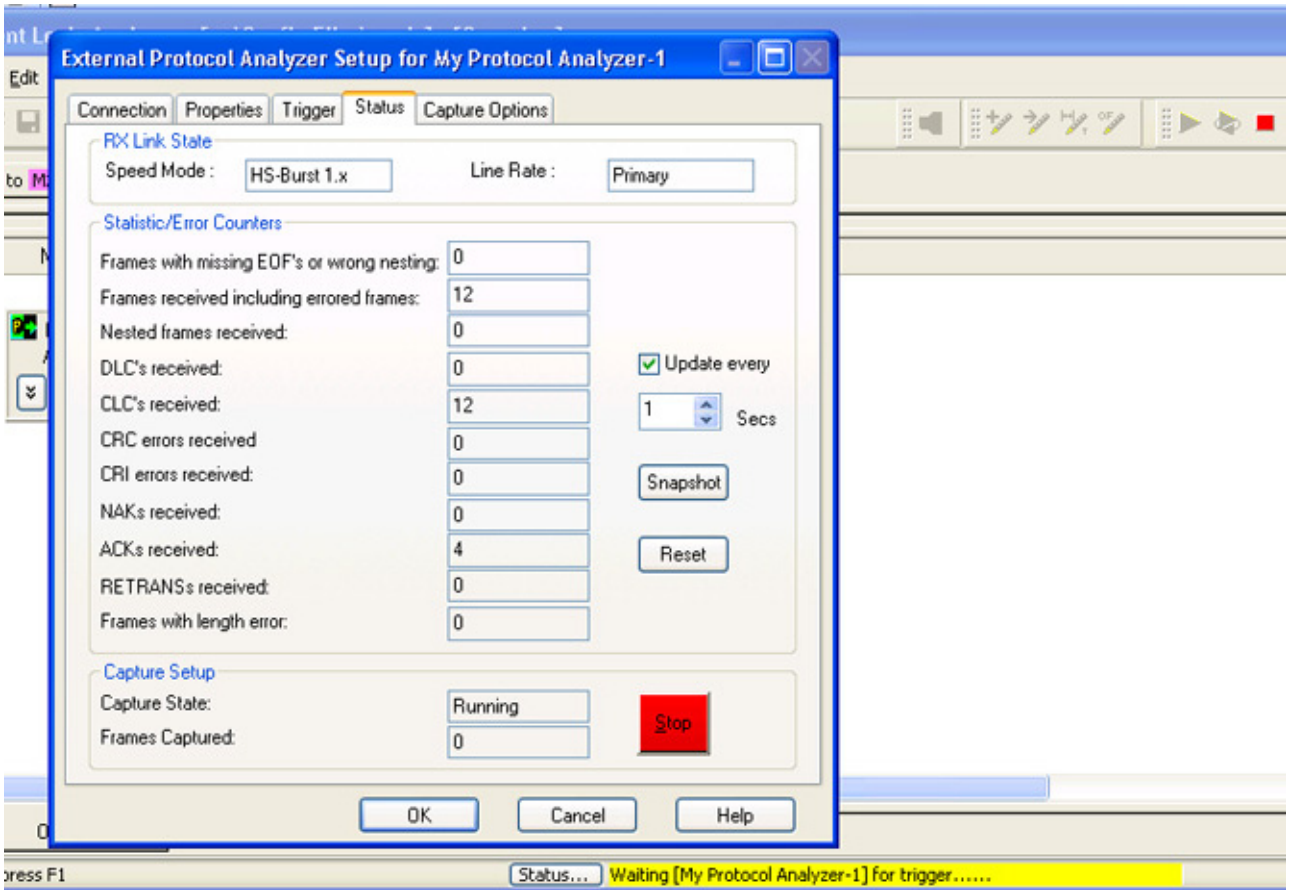


Figure 7 Data capture with ***Go Online*** selected

The Capture State is displayed as Running in the Status tab. The Statistics and error counters for the data capture are simultaneously updated during the capture. However, the total number of frames captured is updated when the data capture stops automatically or you stop it manually. When the data capture stops automatically or manually by either clicking Stop in the Status tab or clicking the **Stop** toolbar button, the data is available in the GUI for display and analysis.

Obtaining/Acquiring the Captured Data

Once the data capture starts using the **Start** button in the **Status** tab, the DigRF Exerciser/ Analyzer module stores the captured data in its memory as per the memory allocation that you configured for the data capture.

To view and analyze the captured data, you need to obtain/acquire the captured data from the DigRF Exerciser / Analyzer memory into Logic Analyzer GUI.

NOTE To obtain/acquire the captured data from the DigRF Exerciser / Analyzer module, a connection (session) is required with the DigRF Exerciser / Analyzer hardware while obtaining the captured data into Logic Analyzer GUI. In the absence of this session, the captured data is not acquired.

To obtain the captured data:

1 Click the **Run** toolbar button from the **Run/Stop** toolbar of the Logic Analyzer GUI. Alternatively, you can also click the **Run Repetitive** toolbar button. Both these buttons perform the same function in case of captured data acquisition from the DigRF Exerciser/Analyzer module.

The **Status** page is displayed with the acquisition details of the captured data. This page is displayed to show the status of acquisition if the data capture is in progress and you have started data acquisition simultaneously or if the data acquisition is in progress.

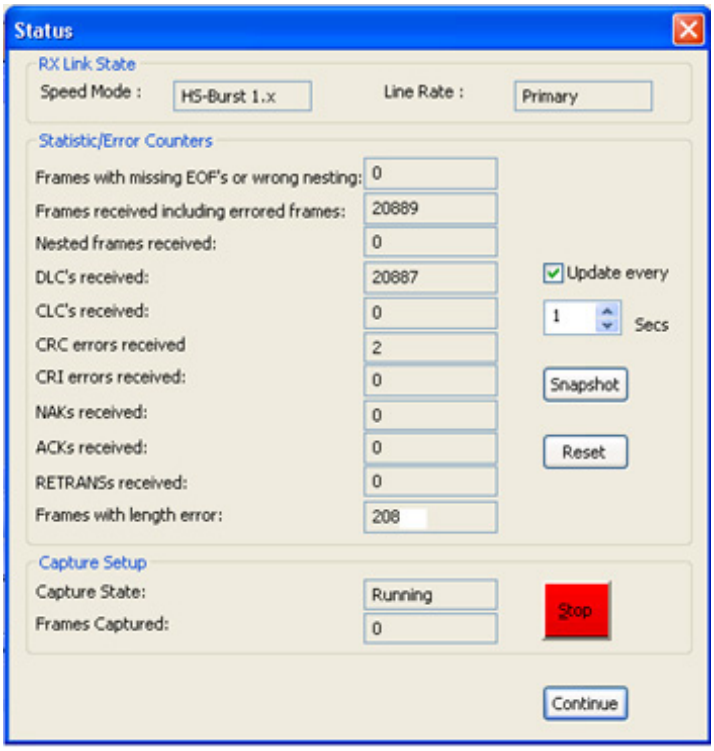


Figure 8 Data acquisition status

All the data captured in the configured direction is acquired from the connected DigRF Exerciser or Analyzer module after which the acquisition stops automatically. Or else, you can also stop the acquisition manually by clicking the Stop button in Status page. The total number of frames acquired is displayed in the **Frames Captured** field after you click Stop to stop the data acquisition process.

Once the data is acquired, you can view it using DigRF tools such as Packet Viewer. Refer to the topic Viewing the Captured DigRF Data Online on page 58 to know more.

NOTE

The acquired data is not displayed for viewing in tools such as Packet Viewer until:

- either the data capture has completed.
- or the data capture/acquisition is manually stopped.

Data Capture and acquisition with the Run toolbar button

The **Run** toolbar button only acquires the already captured data from the connected DigRF Exerciser or Analyzer module. However, you can also use it to perform both the tasks of starting the data capture as well as acquiring the captured data with a single click of this button. To do this, you need to select the **Go online** check box in the **Properties** tab of the External Protocol Analyzer Setup dialog box while configuring the data capture settings.

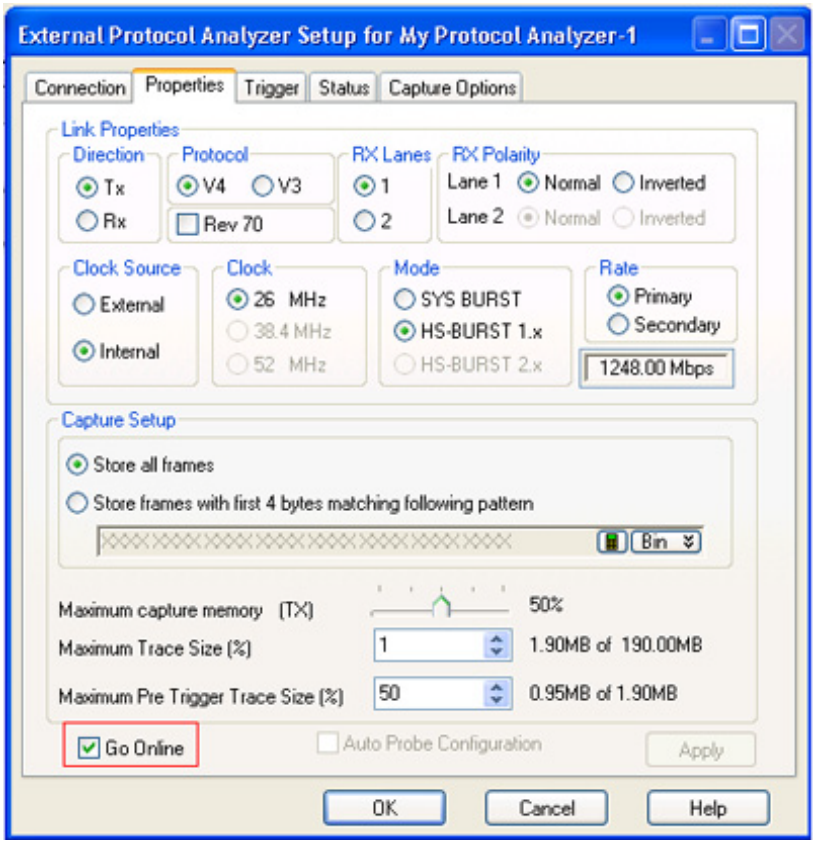


Figure 9 Data capture with the Go online option

Viewing the Captured DigRF Data Online

This topic describes how you can view the data that you captured using either DigRF Exerciser or Analyzer module. Once a session is created and the data is captured and obtained in the Logic Analyzer GUI, you can view this data in the Logic Analyzer GUI. You use the DigRF Analysis tools such as Packet Viewer and Packet Decoder to view the captured data. This data is available for viewing till you do not start the acquisitions of another data capture using the data capture module.

Viewing the unidirectional (Tx or Rx) data capture

In the following example, data sent from BBIC to RFIC (DigRF Exerciser in this case) on the TxData sublink has been captured by adding a data capture module for the Rx side of the DigRF Exerciser.

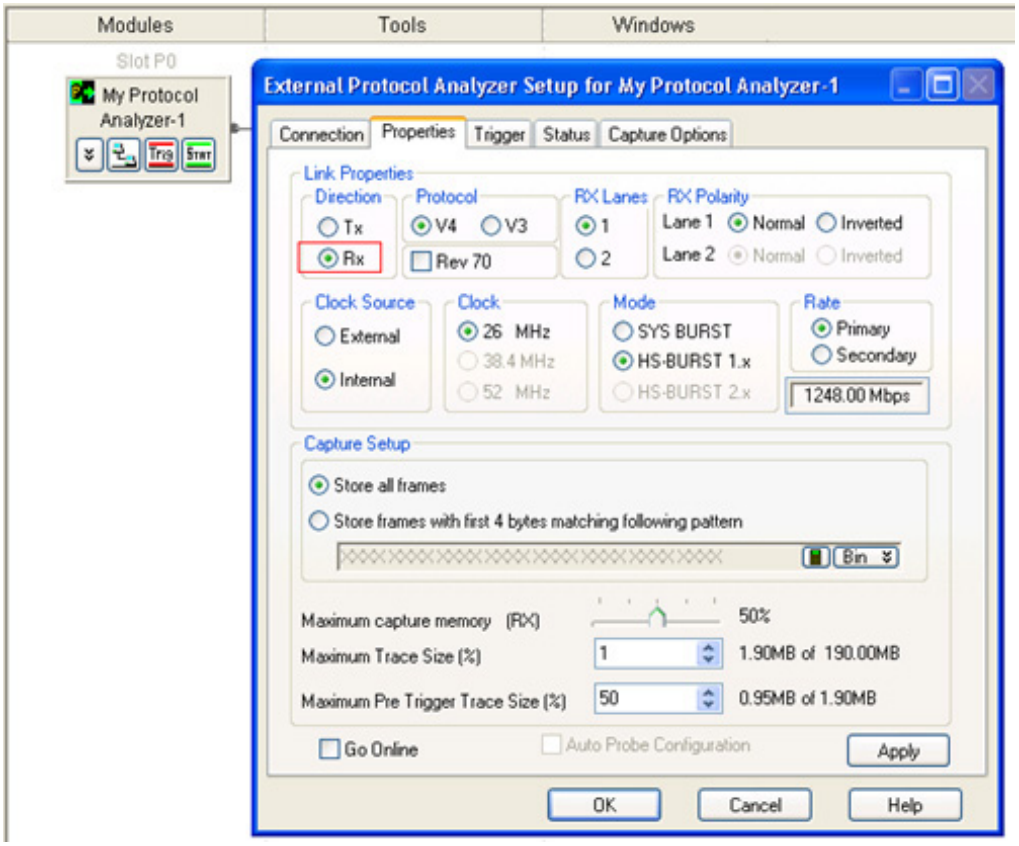


Figure 10 Rx data capture module setup

Using the **Run** toolbar button, the captured data has already been acquired into Logic Analyzer GUI.

To view this acquired data, a Packet Decoder instance is added with the following settings to decode the captured Tx packets that is, packets sent from BBIC to DigRF Exerciser on the TxData sublink. Notice that the Decode bus has been selected as Tx.

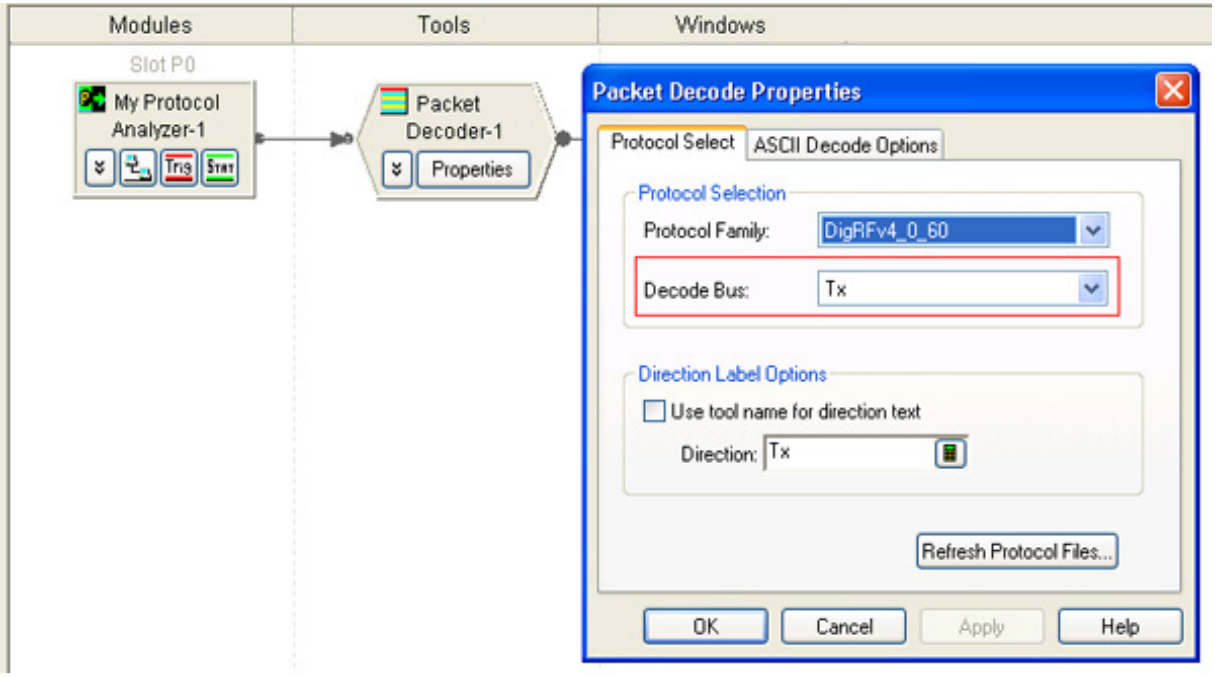


Figure 11 Packet Decoder for the captured Tx packets

To view the decoded Tx packets, a Packet Viewer instance has been added to the Packet Decoder instance. To view the decoded Rx packets as waveforms, the waveform view has been added to the Packet Decoder instance.

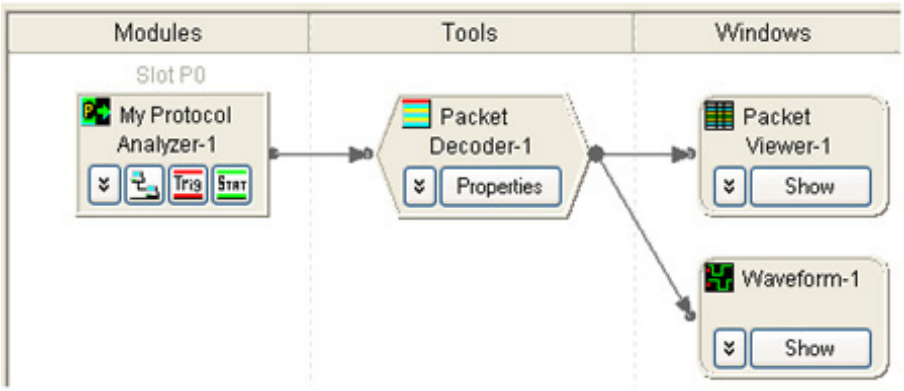


Figure 12 Waveform and Packet Viewer for viewing captured data

The captured Tx packets are displayed in the following screen using Packet Viewer.

Packets

Sample Number	Direction	CRI	DigRFv4_0_60 Packet	ICLC Command	ICL
-106	Tx	0101	Tx Interface Control Logical Channel	Ping Request	
-99	Tx	0110	Tx Interface Control Logical Channel	Tx Data Sub-Link Rate	
-92	Tx	0111	Tx Interface Control Logical Channel	Rx Data Sub-Link Rate	
-85	Tx	1000	Tx Acknowledge Control Logical Channel		
-81	Tx	1001	Data Logical Channel 0		
-46	Tx	1011	Data Logical Channel 0		
-11	Tx	0000	Tx Interface Control Logical Channel	Dummy Frame	
-4	Tx	0001	Tx Acknowledge Control Logical Channel		

Figure 13 Captured data displayed in Packet Viewer

Viewing the bidirectional data capture

The following is an example of how you can view the data captured in both Tx and Rx directions (dual capture).

In this example, the following data capture module has been added to capture the data sent from the BBIC (DigRF Exerciser in this case) to RFIC. This data capture module captures the Tx side of DigRF Exerciser.

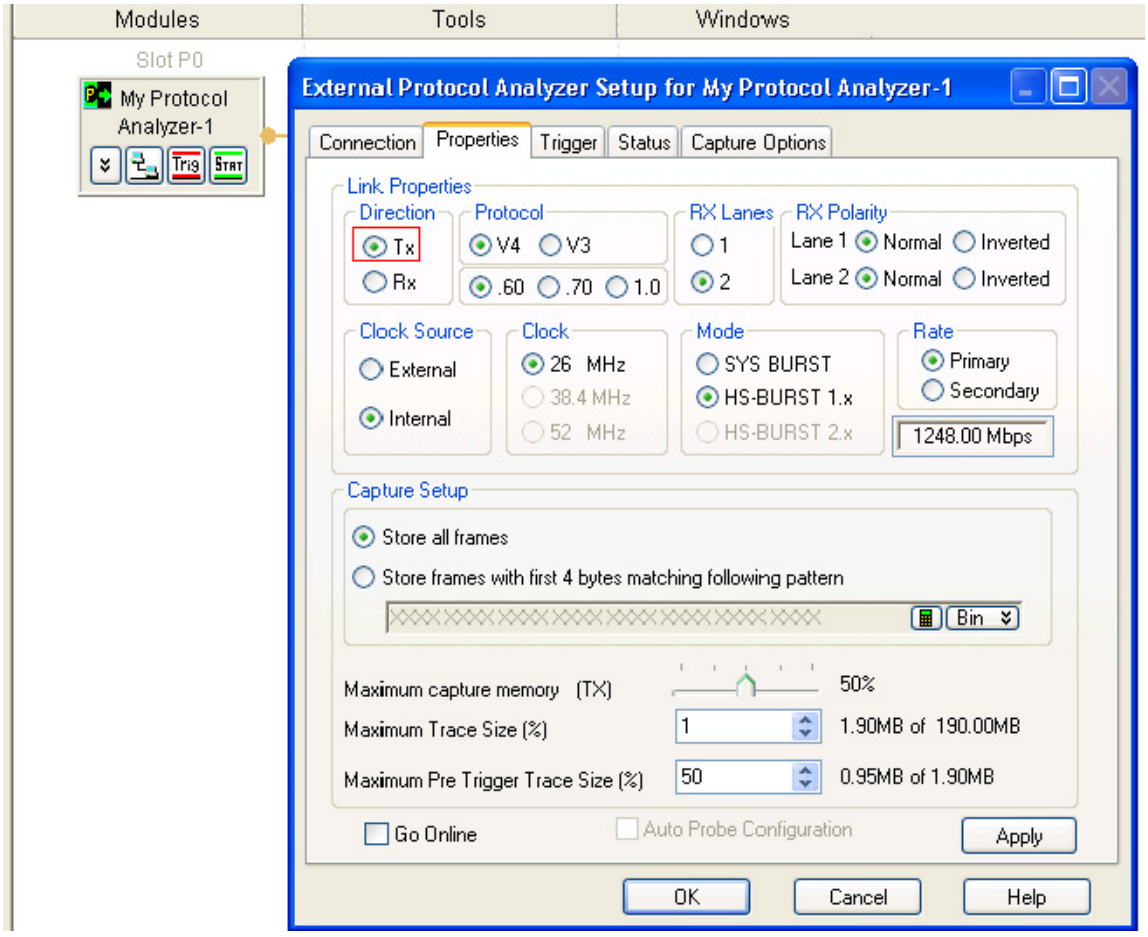


Figure 14 Tx data capture module setup

Another data capture module has been added to capture the data sent from RFIC to BBIC (DigRF Exerciser in this case). This data capture module captures the Rx side of DigRF Exerciser.

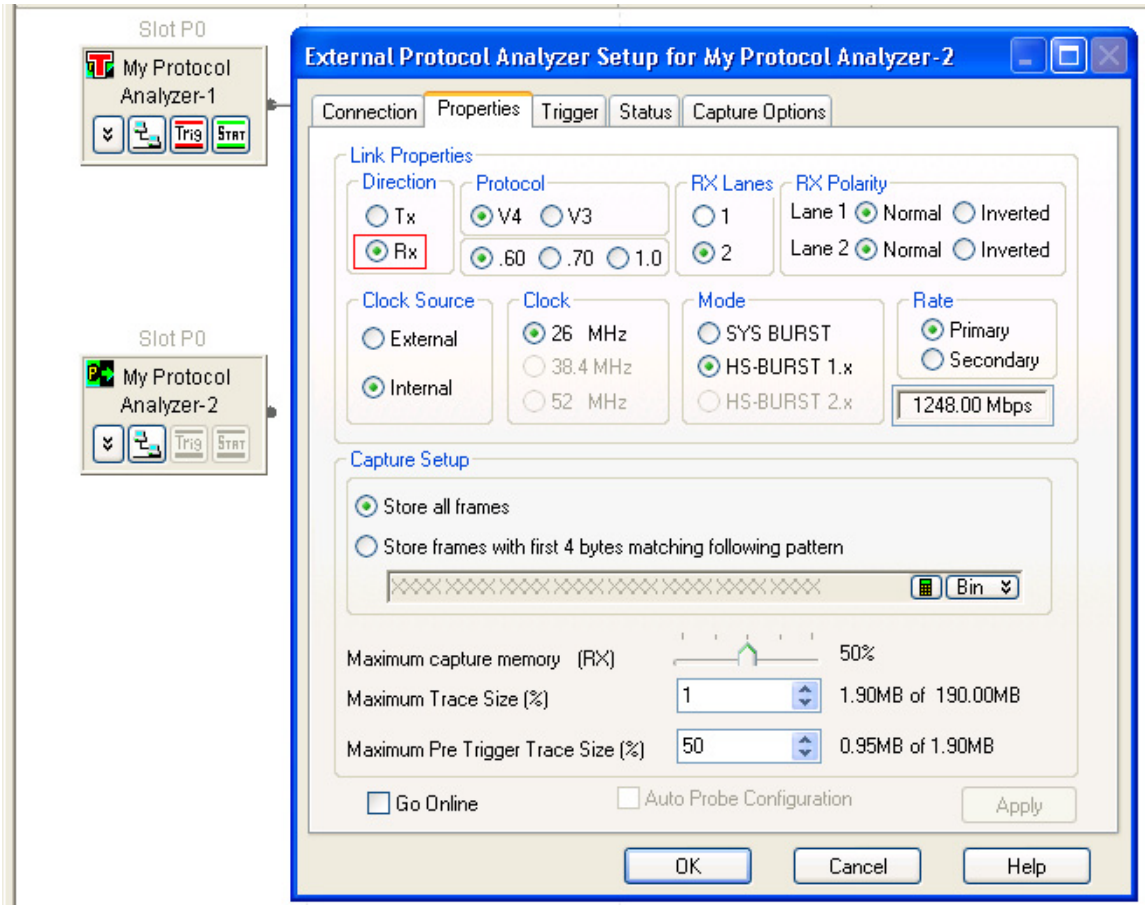


Figure 15 Rx data capture module

Using the **Run** toolbar button, the Tx and Rx data have already been acquired into Logic Analyzer GUI.

To view the acquired Tx and Rx data, two Packet Decoder instances are added to decode the data captured in the Tx and Rx directions of DigRF Exerciser. The Decode bus has been selected as Tx for the Packet Decoder instance that decodes the Tx packets, that is, packets sent on the TxData sublink from DigRF Exerciser to RFIC. For the other Packet Decoder instance, the Decode bus has been selected as Rx to decode the Rx packets that is, packets sent on the RxData sublink from RFIC to DigRF Exerciser.

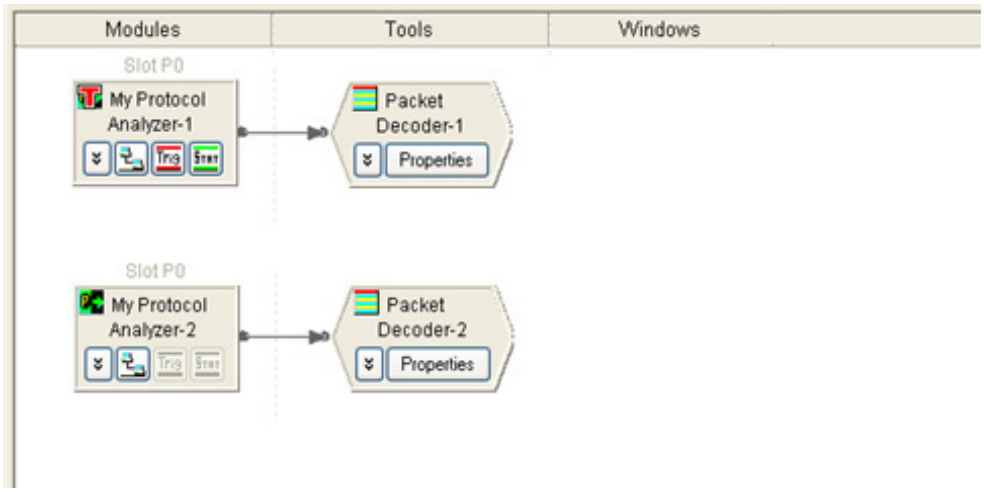


Figure 16 Packet Decoders to decode the captured Tx and Rx packets

To view the decoded Tx and Rx data in co-relation to each other, both the Rx and Tx Packet Decoder instances are pointed to the same Packet Viewer window.

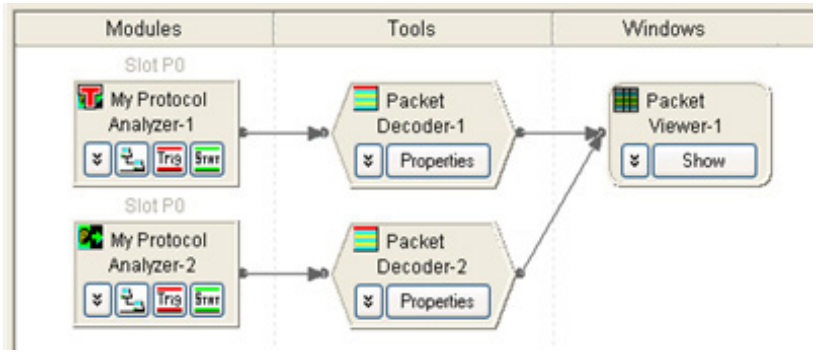


Figure 17 Single Packet Viewer for both Tx and Rx packets

The Packet Viewer window displays the decoded Rx packets in relation to the Tx packets exchanged over the link.

Packets

Sample Number	Direction	CRI	DigRFv4_0_60 Packet	ICLC C
-280	Tx	0100	Tx Interface Control Logical Channel	
-55	Rx	0100	Rx Acknowledge Control Logical Channel	
-51	Rx	0101	Rx Interface Control Logical Channel	
-273	Tx	0101	Tx Acknowledge Control Logical Channel	
-269	Tx	0110	Data Logical Channel 0	
-44	Rx	0110	Rx Acknowledge Control Logical Channel	
-234	Tx	1011	Data Logical Channel 0	
-199	Tx	1000	Tx Interface Control Logical Channel	
-40	Rx	0111	Rx Acknowledge Control Logical Channel	
-36	Rx	1000	Rx Acknowledge Control Logical Channel	
-192	Tx	1001	Data Logical Channel 0	
-32	Rx	1001	Rx Acknowledge Control Logical Channel	
-125	Tx	1011	Data Logical Channel 0	
-58	Tx	0000	Tx Interface Control Logical Channel	
-28	Rx	1010	Rx Acknowledge Control Logical Channel	
-24	Rx	0000	Rx Acknowledge Control Logical Channel	
-51	Tx	0001	Data Logical Channel 0	

Figure 18 Correlated bi-directional data

Viewing the Captured Data Offline

In RDX test platform, the Logic Analyzer GUI is used to configure the link and data capture setup and to start the data capture using either DigRF Exerciser or Analyzer module. In this mode, a connection is needed between the Logic Analyzer GUI and the DigRF Exerciser or Analyzer hardware to control the capture and then obtain the captured data for viewing in Logic Analyzer GUI.

However, once you have obtained the captured data from the DigRF Exerciser or Analyzer module into the Logic Analyzer GUI, you can view this data offline. Offline here means no connection is needed between the Logic Analyzer GUI and the DigRF Exerciser or Analyzer hardware to view the captured data. To accomplish this:

1 Configure the settings to save the captured data in a file while acquiring it into Logic Analyzer GUI.

2 Import the saved file in the Logic Analyzer GUI.

3 View and analyze it offline using the DigRF Analysis tools.

Saving the captured data

You can perform the following steps to ensure that the data acquired from the DigRF Exerciser/Analyzer module is saved automatically in the specified file after the data acquisition is complete.

1 Select **Run/Stop > Run Properties** menu option from the Logic Analyzer GUI main menu.

The **Run Properties** dialog box is displayed.

2 Select the **Save after every acquisition** check box.

3 In the **Base file name** field, specify the full path and name of the file in which you want to save the acquired data.

4 Select the **Module CSV text file (*.csv)** option from the **Save as type** listbox.

5 Click **Settings** and then select the source from which the captured data should be saved. For instance, if you have added a Tx and Rx module for data capture in Logic Analyzer GUI, then you can select the source as one of these modules to save the data captured using the selected module.

6 Click **OK**.

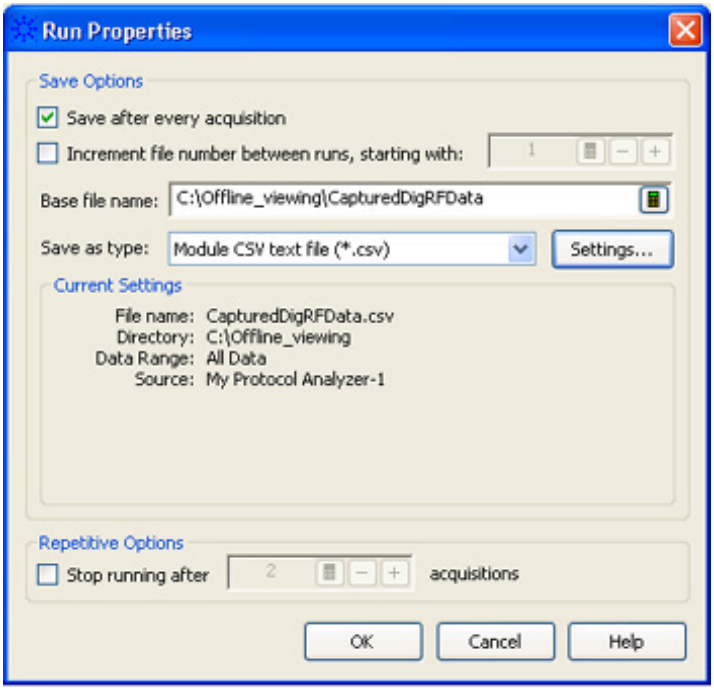


Figure 19 Settings for saving the captured data

After configuring these settings, the captured data from the specified source will automatically be saved at the specified path and file when you obtain the captured data using the **Run** button in Logic Analyzer.

Importing the saved file

NOTE To import the captured data from the saved module CSV text file into Logic Analyzer GUI, you need the Data_Import license.

You can import the saved module CSV text file into the Logic Analyzer GUI to view the data offline. To do this:

1. Launch the Logic Analyzer GUI.
2. Click **File** -> **Import**.

   The **Import** dialog box is displayed.
3. Select **Module CSV Text File** as the file type to be imported and click **OK**.
4. Browse and select the module CSV text file that you want to import and click **Import**.

The file is imported as a Data Import module in the Overview tab of the Logic Analyzer GUI. You can then add the required tools and windows to this module to view and analyze the imported data offline. To know about the tools, refer to Introduction to DigRF Analysis Tools on page 83.

The following screen displays a module CSV text file imported as a Data Import module in Logic Analyzer GUI. Packet Decoder and Packet Viewer have been added to decode and view the imported data.

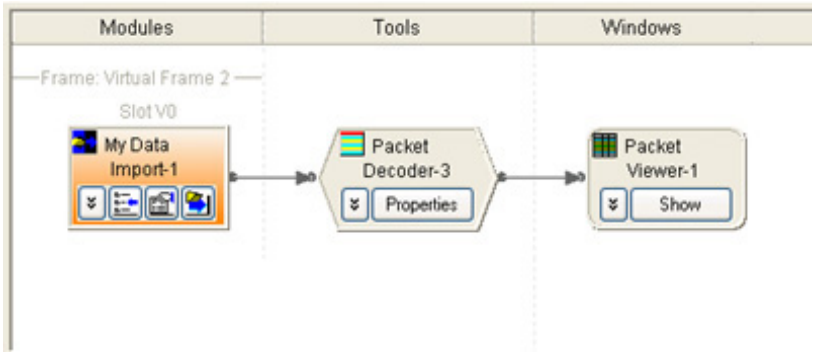
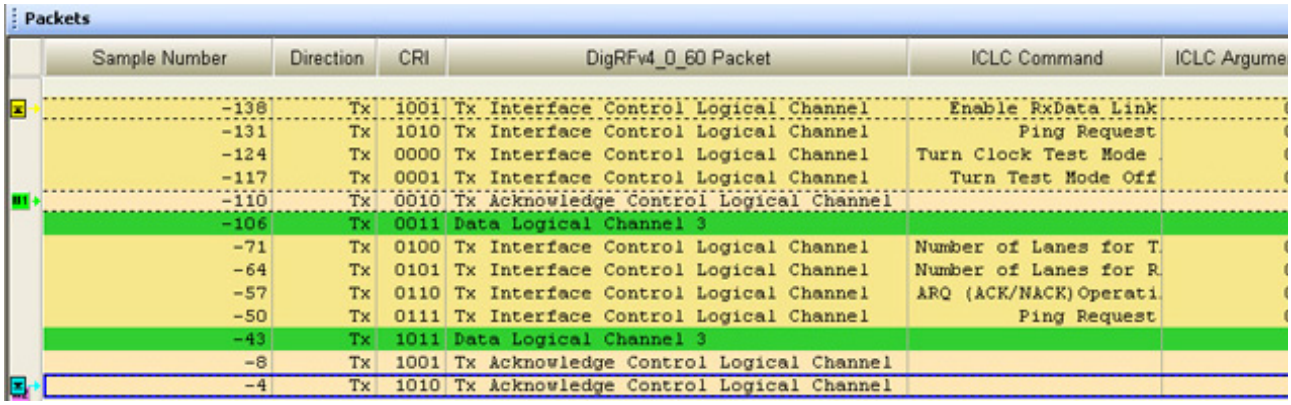


Figure 20 Imported data module

The following screen displays the DigRF data from this data import module in Packet Viewer for offline viewing and analysis.



Sample Number	Direction	CRI	DigRFv4_0_60 Packet	ICLC Command	ICLC Argume
-138	Tx	1001	Tx Interface Control Logical Channel	Enable RxData Link	
-131	Tx	1010	Tx Interface Control Logical Channel	Ping Request	
-124	Tx	0000	Tx Interface Control Logical Channel	Turn Clock Test Mode	
-117	Tx	0001	Tx Interface Control Logical Channel	Turn Test Mode Off	
-110	Tx	0010	Tx Acknowledge Control Logical Channel		
-106	Tx	0011	Data Logical Channel 3		
-71	Tx	0100	Tx Interface Control Logical Channel	Number of Lanes for T	
-64	Tx	0101	Tx Interface Control Logical Channel	Number of Lanes for R	
-57	Tx	0110	Tx Interface Control Logical Channel	ARQ (ACK/NACK) Operati	
-50	Tx	0111	Tx Interface Control Logical Channel	Ping Request	
-43	Tx	1011	Data Logical Channel 3		
-8	Tx	1001	Tx Acknowledge Control Logical Channel		
-4	Tx	1010	Tx Acknowledge Control Logical Channel		

Figure 21 Viewing data offline

You can also perform offline RF analysis of the saved data using VSA. Refer to the topic Analyzing Captured Data using VSA on page 93 to know more.

Example - DigRF Data Capture

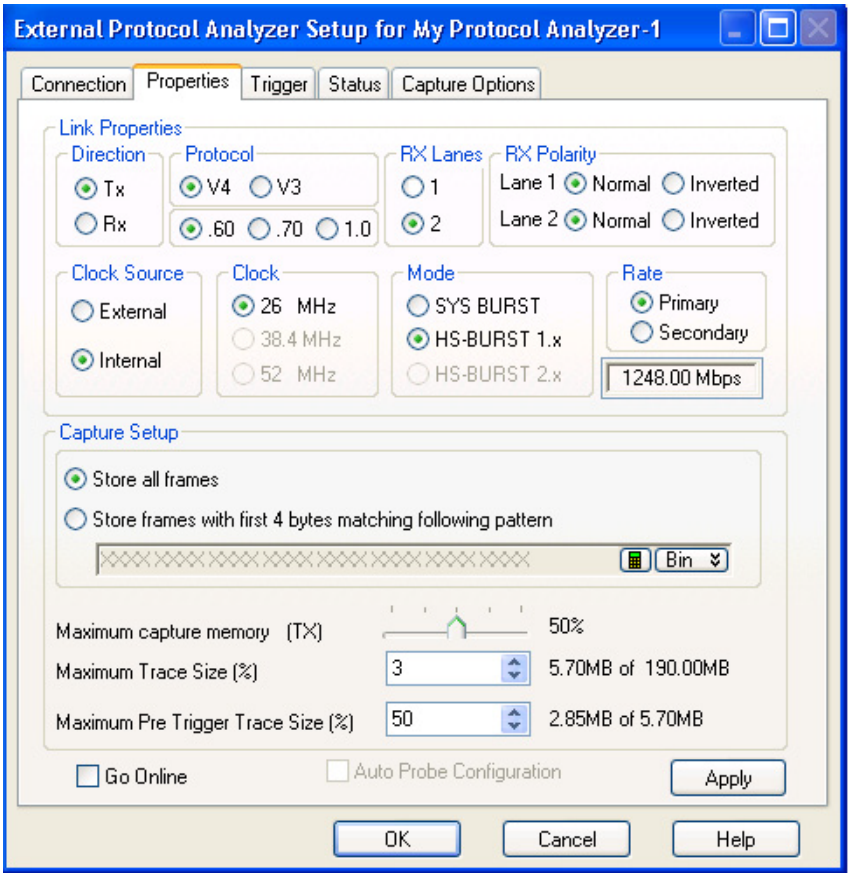
This topic provides an example of a DigRF data capture flow created and executed using the Logic Analyzer GUI. The data capture is done using the DigRF Exerciser module in this example.

DigRF Data Capture using the Logic Analyzer GUI

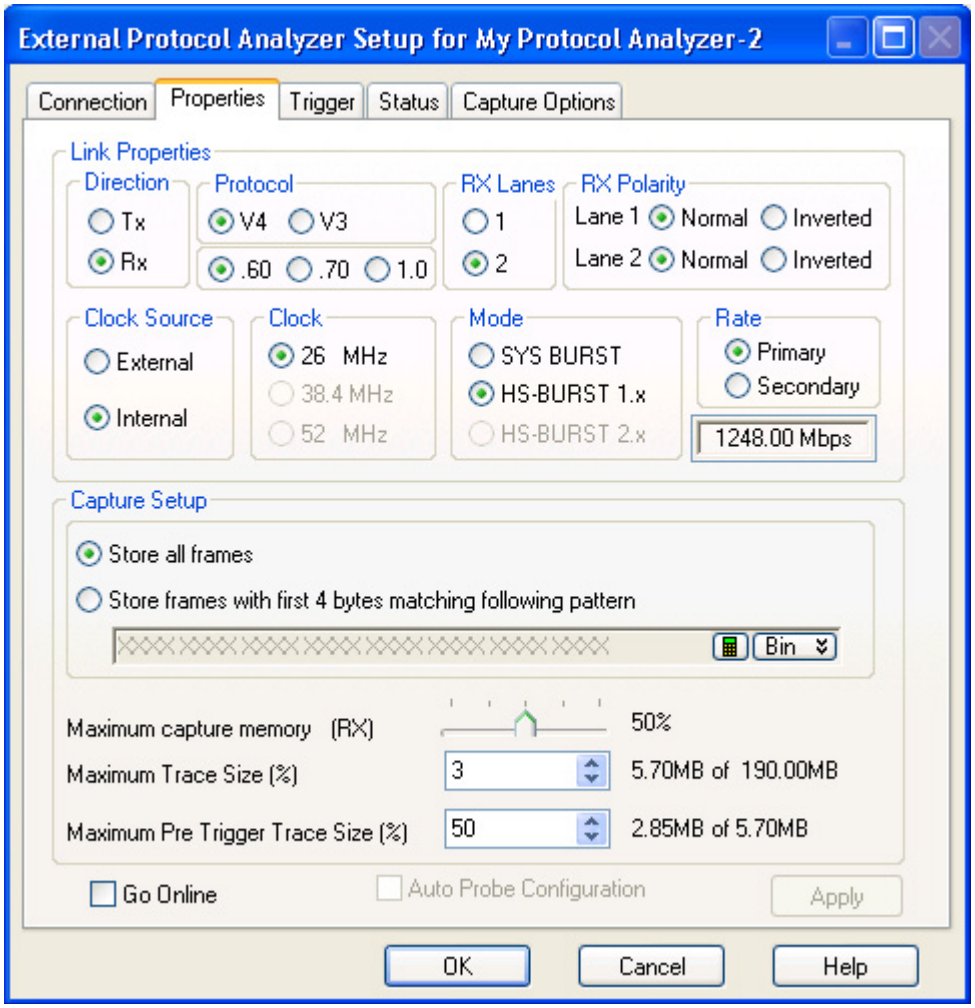
This example focuses on the testing of a BBIC independent of an RFIC. DigRF Exerciser is emulating the missing link partner - RFIC and is used for sending stimulus to BBIC (DUT). The stimulus flow is already set using the Protocol Exerciser for DigRF GUI. In the following sections, the data capture flow is set to capture the Tx and Rx data exchanged between BBIC and DigRF Exerciser over the configured DigRF link. The data received from BBIC (DUT) should start getting captured when it sends a **Number of Lanes for TxData sublink** frame to DigRF Exerciser emulating an RFIC.

Link configuration for the data capture

To capture data both ways, the following two modules have been set up in Logic Analyzer GUI. The Tx module captures the data transmitted by DigRF Exerciser, that is, RFIC in this case, it captures the data sent by DigRF Exerciser (RFIC) on the RxData sublink. Notice the link direction has been set to Tx.

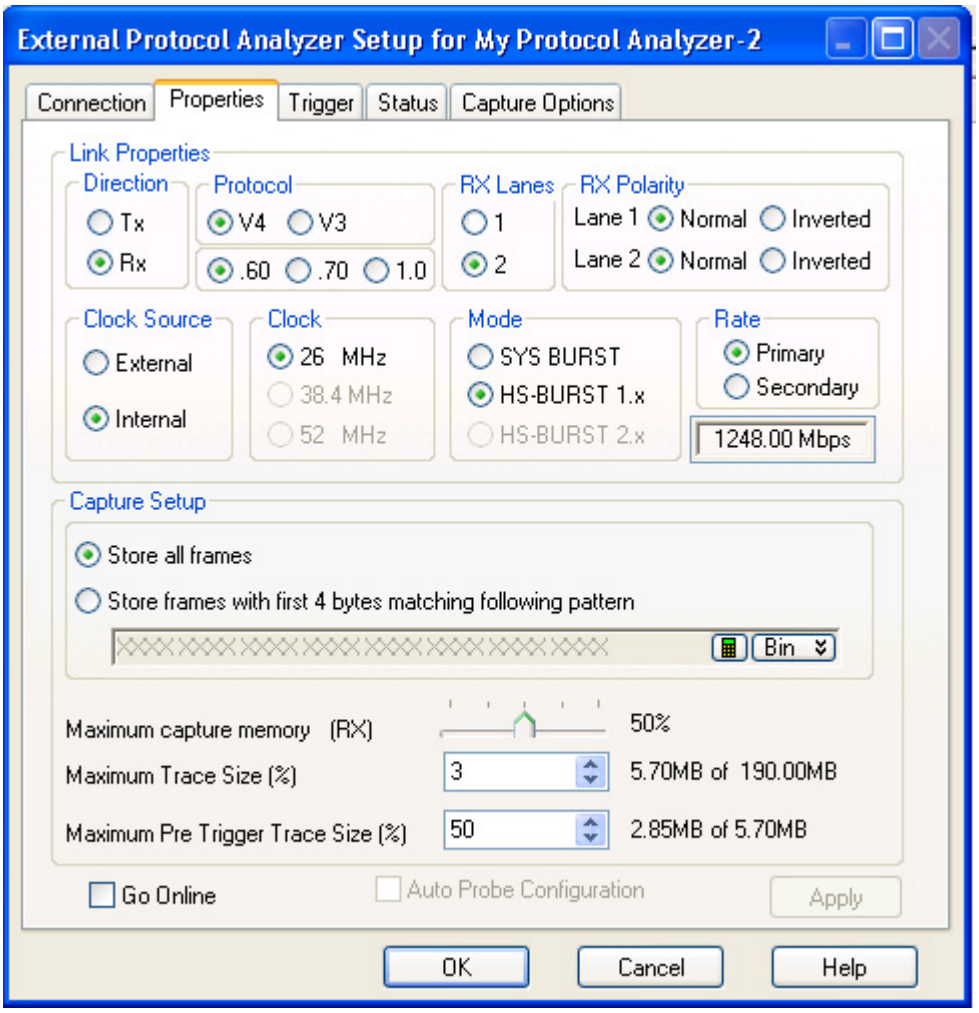


The Rx module captures the data received by DigRF Exerciser, that is, in this case, it captures the data received by DigRF Exerciser (RFIC) on the TxData sublink. Notice the link direction has been set to Rx.



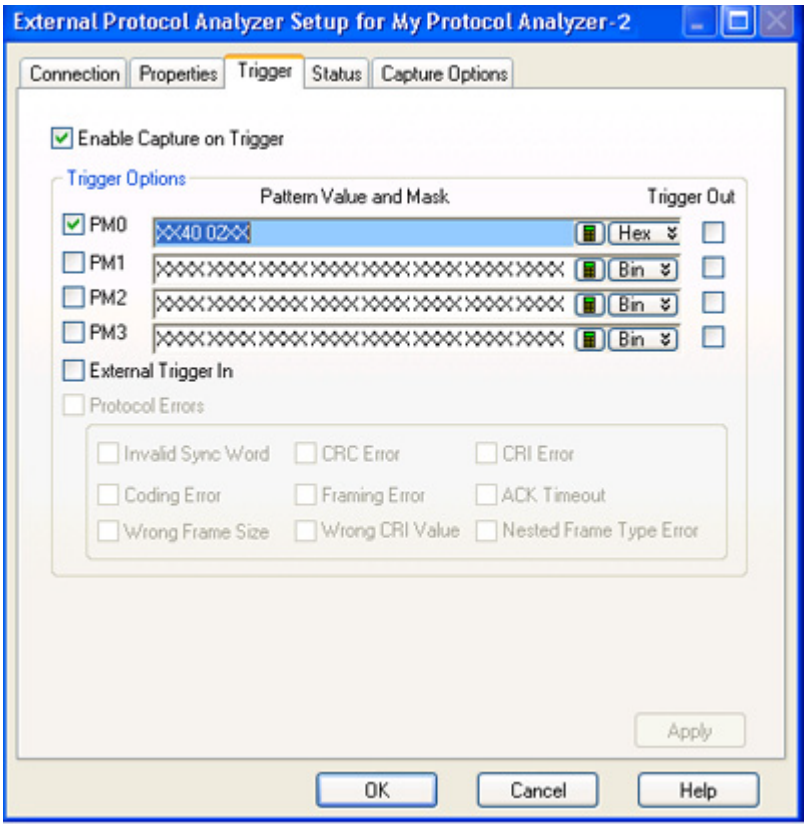
DigRF Exerciser Capture Setup

The DigRF Exerciser module is capturing data both ways. Therefore, the capture memory is divided equally between the Tx and Rx captures. The allocated capture memory for Rx is further divided into pre trigger and post trigger capture memory.



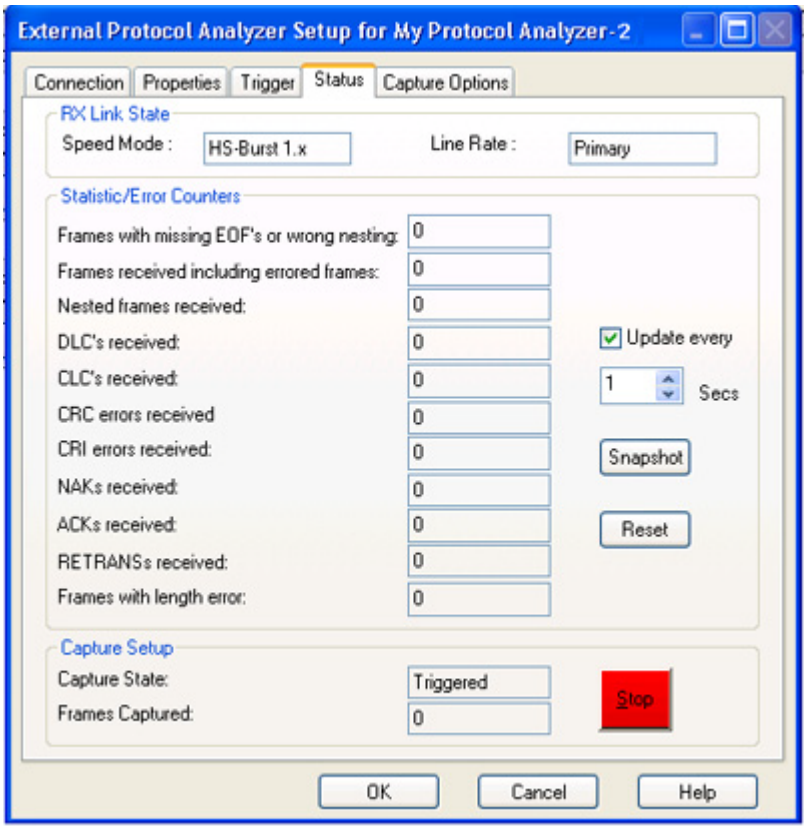
Setting Trigger to start capture on the Rx side of DigRF Exerciser

The data received from BBIC (DUT) should start getting captured when it sends the **Number of Lanes on the TxData sublink** frame to DigRF Exerciser emulating an RFIC. To accomplish this, a capture trigger is enabled on the Rx data capture, that is the data received by DigRF Exerciser from BBIC. The following screen displays the pattern value **XX4002XX** Hex specified for this trigger. The value has been specified matching the payload of the Number of Lanes on the TxData sublink frame. The first byte, **XX** is for the header of the frame and **4002XX** are for the payload of the frame. On encountering a frame matching this pattern, the data capture should start.



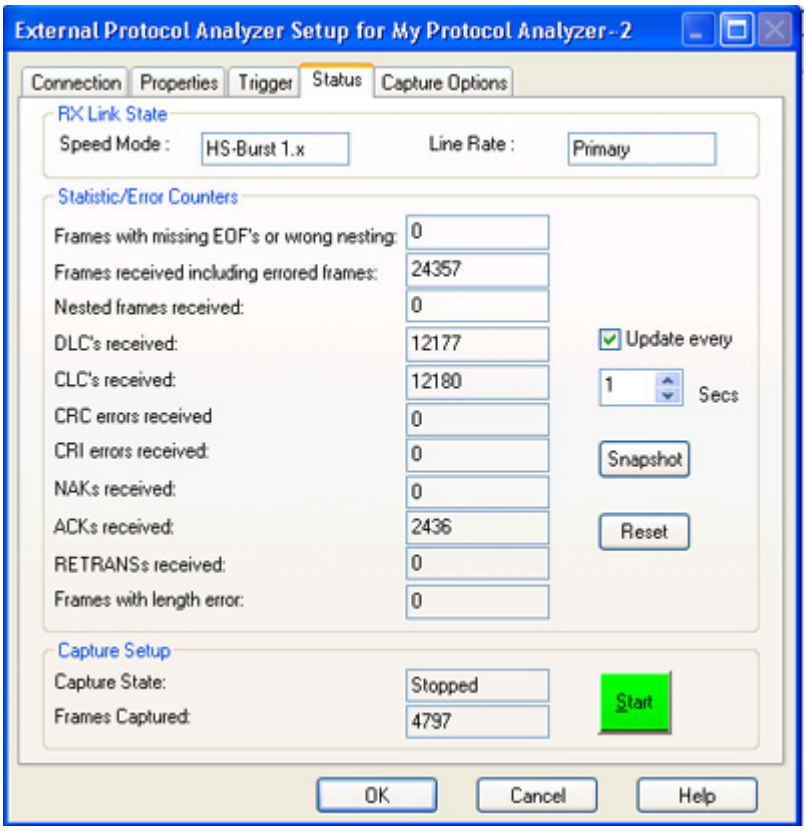
Starting the capture and stimulus

First, data capture is started as per the capture settings by clicking the **Start** button in the External Protocol Analyzer Setup dialog box. The capture state is displayed as **Triggered** representing that a trigger condition has been set for the data capture.



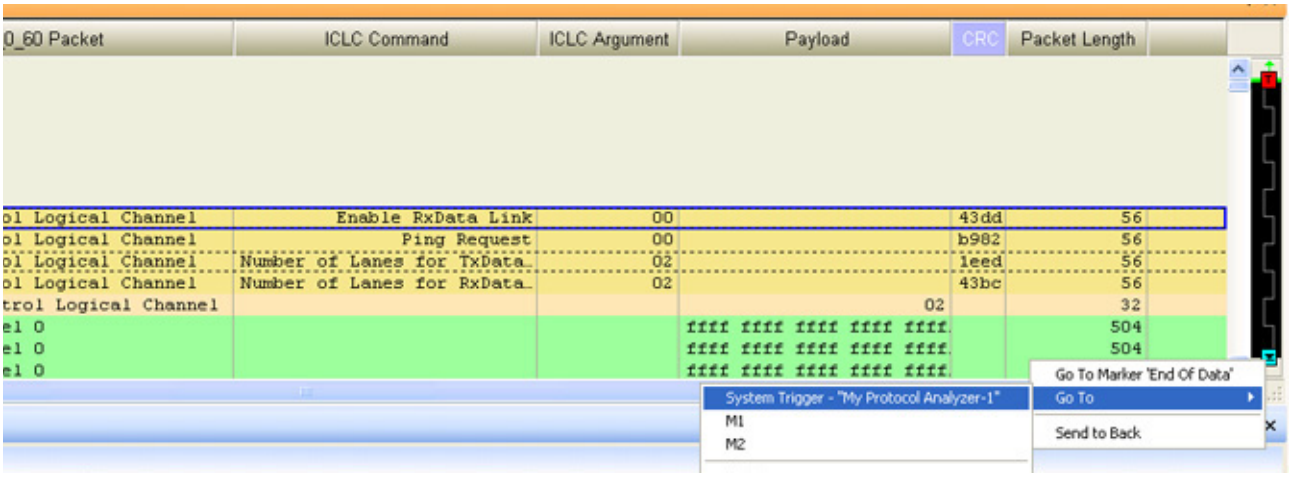
Next, the stimulus flow is started in the Protocol Exerciser for DigRF GUI as per the configured stimulus flow. On starting the stimulus, the capture state is displayed as **Running**. The frames received from BBIC are checked against the trigger conditions. When a Number of Lanes on the TxData sublink frame is received from DUT, the frames are captured in the post trigger memory of DigRF Exerciser.

The capture stops automatically when the allocated post trigger capture memory is full. The total number of frames captured is also displayed.

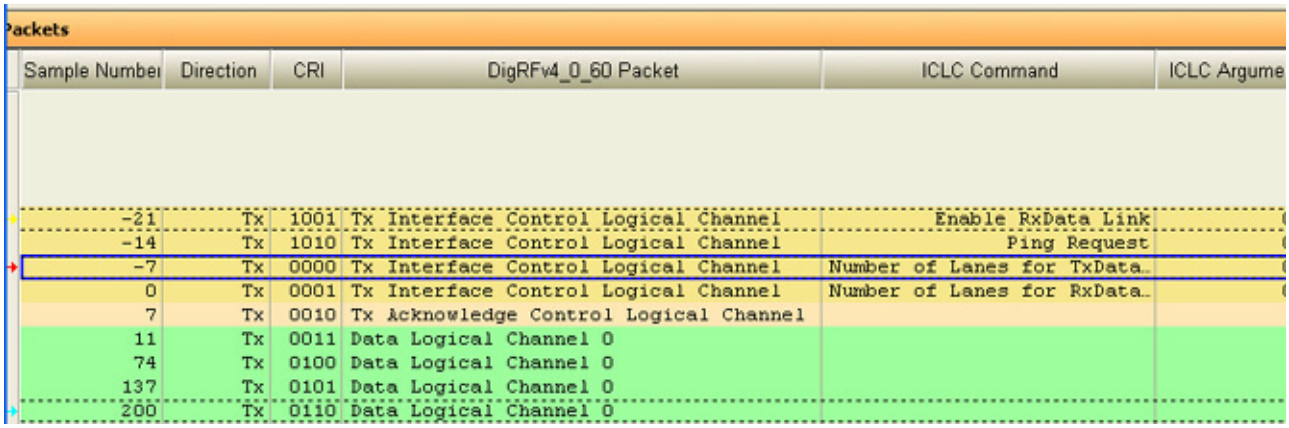


Viewing the captured data

The captured Tx and Rx data is obtained in the Logic Analyzer GUI by clicking the **Run** toolbar button. The Packet Viewer displays both the pre trigger and post trigger data captured on the receiver side of DigRF Exerciser. To view the frame from which the trigger condition is met and data started getting captured in post trigger memory, right-click the Trigger marker in the upper pane of Packet Viewer. Then select **Go To** and then select **System Trigger**.



Clicking the System trigger option highlights the frame that triggered the data capture. Notice that the **Number of Lanes on the TxData sublink** frame is highlighted as the frame that triggered the data capture.



For the data captured on the Transmitter side of Exerciser, no trigger condition was set. Therefore, all the captured data is displayed in the Packet Viewer without the trigger position.

Packets

Sample Number	Direction	CRI	DigRFv4_0_60 Packet	ICLC Command	ICLC Argument
-12952	Rx	0111	Rx Acknowledge Control Logical Channel		
-12948	Rx	1000	Rx Interface Control Logical Channel	Ping Response	a5
-12941	Rx	1001	Rx Acknowledge Control Logical Channel		
-12937	Rx	1010	Rx Acknowledge Control Logical Channel		
-12933	Rx	0000	Rx Acknowledge Control Logical Channel		
-12929	Rx	0001	Rx Acknowledge Control Logical Channel		
-12925	Rx	0010	Rx Acknowledge Control Logical Channel		
-12921	Rx	0011	Rx Interface Control Logical Channel	Ping Response	a5
-12914	Rx	0100	Rx Acknowledge Control Logical Channel		
-12910	Rx	0101	Rx Acknowledge Control Logical Channel		
-12906	Rx	0110	Rx Acknowledge Control Logical Channel		
-12902	Rx	0111	Rx Acknowledge Control Logical Channel		
-12898	Rx	1000	Rx Acknowledge Control Logical Channel		
-12894	Rx	1001	Rx Interface Control Logical Channel	Ping Response	a5
-12887	Rx	1010	Rx Acknowledge Control Logical Channel		

Performing DigRF Protocol Level Testing

Testing ACK/NACK Mechanisms

You can use DigRF Exerciser's stimulus and capture capabilities to test if the DUT's ACK/NACK mechanisms are accurately implemented to ensure data transfer reliability over the DigRF link.

Viewing ACK/NAK Statistics

You can check the number of ACK and NACK responses received from DUT by viewing the status information in the Status tab of the External Protocol Analyzer Setup dialog box. The following screen displays this information in the Status page in the Logic Analyzer GUI.

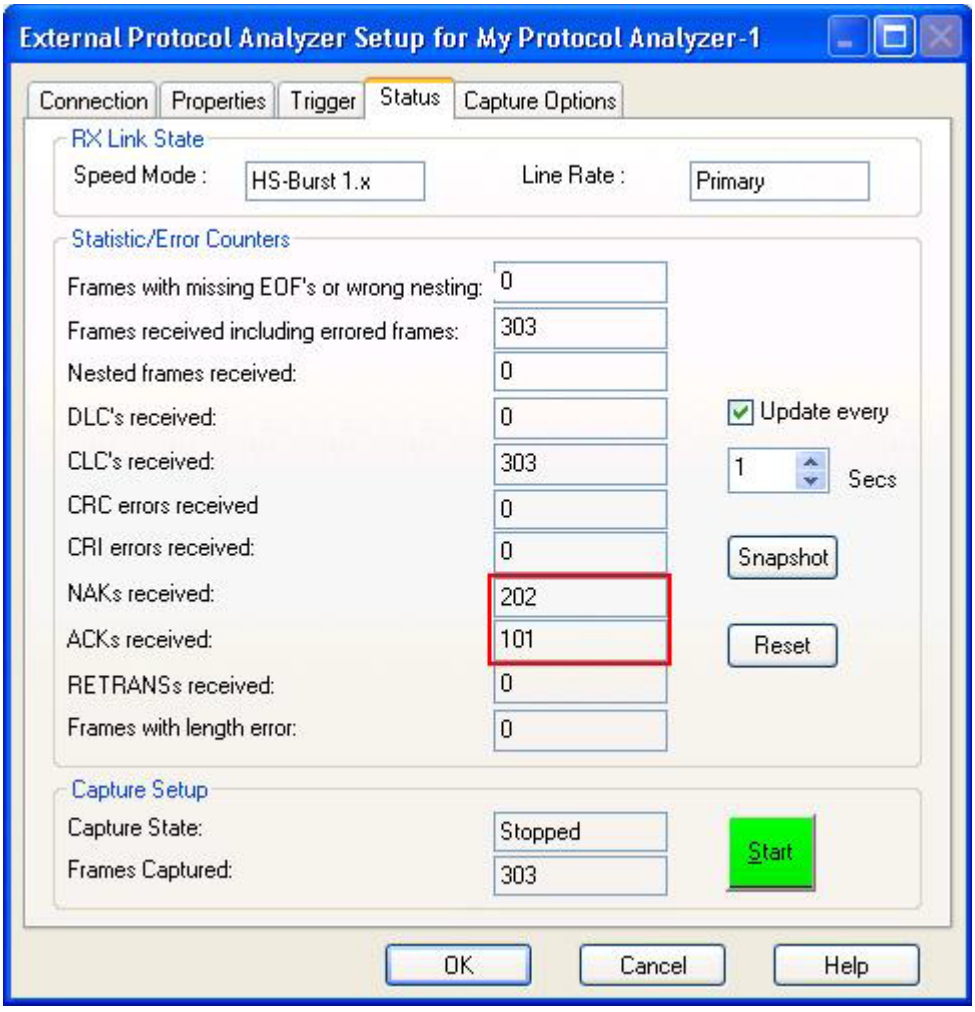


Figure 22 ACK/NAK statistics

You can also view the number of ACK/NACK received from DUT in the capture flow configured in the Logic Analyzer GUI. Using the bidirectional data capture, you can view the packet sent to DUT and the ACK/NACK received from DUT as response in the Packet Viewer.

Packets

Sample Number	Direction	CRI	DigRFv4_0_60 Packet	ICLC C
-260	Tx	0100	Tx Interface Control Logical Channel	
-55	Rx	0100	Rx Acknowledge Control Logical Channel	
-51	Rx	0101	Rx Interface Control Logical Channel	
-273	Tx	0101	Tx Acknowledge Control Logical Channel	
-269	Tx	0110	Data Logical Channel 0	
-44	Rx	0110	Rx Acknowledge Control Logical Channel	
-234	Tx	1011	Data Logical Channel 0	
-199	Tx	1000	Tx Interface Control Logical Channel	
-40	Rx	0111	Rx Acknowledge Control Logical Channel	
-36	Rx	1000	Rx Acknowledge Control Logical Channel	
-192	Tx	1001	Data Logical Channel 0	
-32	Rx	1001	Rx Acknowledge Control Logical Channel	
-125	Tx	1011	Data Logical Channel 0	
-58	Tx	0000	Tx Interface Control Logical Channel	
-28	Rx	1010	Rx Acknowledge Control Logical Channel	
-24	Rx	0000	Rx Acknowledge Control Logical Channel	
-51	Tx	0001	Data Logical Channel 0	
-36	Tx	0010	Tx Interface Control Logical Channel	Tx
-29	Tx	0011	Tx Interface Control Logical Channel	Number of Lanes :
-20	Rx	0001	Rx Acknowledge Control Logical Channel	

Figure 23 ACK/NAK captured

Testing ACK/NACK responses from DUT

You can use DigRF Exerciser to test if a DUT sends ACK/NACK in response to the stimulus frames. For instance, you can send a frame with 8B/10B (Disparity) error as stimulus to DUT. By capturing data sent by DUT, you can check if the DUT responds with a NACK to this errored frame.

You can also configure dual capture (capturing the Tx and Rx data over the link) to view the ACK or NACK response received in relation to the errored frame sent as stimulus.

The following screen displays the output of such a dual capture scenario where an errored data frame is sent to DUT and a NACK is received from DUT in response.

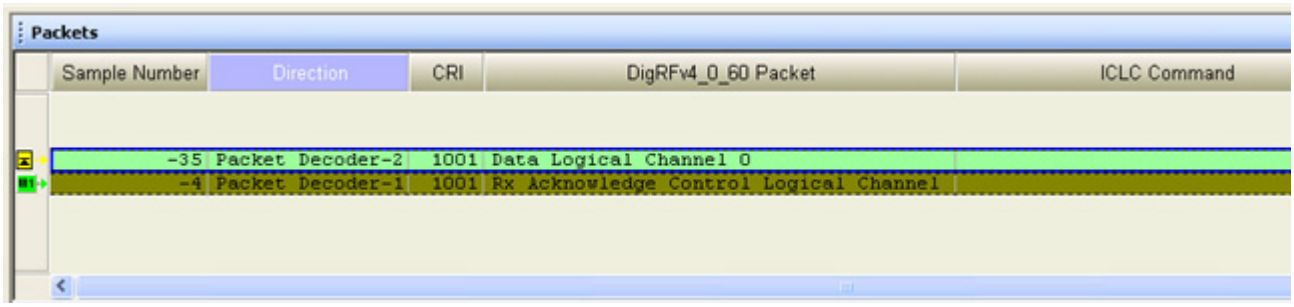


Figure 24 NAK captured

To know how to send an errored frame as stimulus, refer to the online help of the Protocol Exerciser for DigRF GUI and to capture Tx and Rx data simultaneously, refer to Configuring a Dual Capture Setup on page 44.

Testing DUT's responses to ACK/NACK

You can also test how the DUT responds to the ACK/NACK received from DigRF Exerciser. For instance, you can test if the DUT responds to a NACK received from DigRF Exerciser by retransmitting the frame. Refer to the topic Testing Frame Retransmission on page 80 to know more.

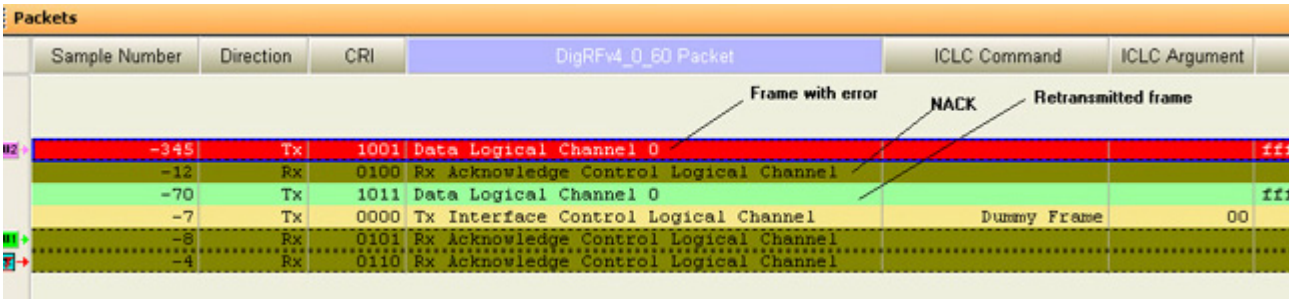
Testing Frame Retransmission

You can test how the DUT handles the retransmission of frames over the DigRF link.

Testing retransmission of frames from DUT

For the errored frames received from DUT, DigRF Exerciser sends NACKs to DUT. You can then capture the data received from DUT to check the retransmission of the frame for which DigRF Exerciser sent a NACK.

The following screen displays a capture sequence of an errored frame received from DUT on TxData sublink, followed by a NACK from Exerciser and then the retransmission from DUT.



Further, you can validate the structure of the retransmitted frame received from DUT. Refer to the topic Validating a DigRF Frame Structure on page 88 to know how you can validate the structure of a retransmitted frame captured over the DigRF link.

Detecting Protocol Violations in Received DigRF Frames

You can detect if there are any DigRF protocol violations in the frames received from the DUT. To do this, you can configure settings in the Logic Analyzer GUI to ensure that DigRF Exerciser/Analyzer checks the captured data and control frames from the DUT for protocol violations. On encountering a protocol violation in the received frames, it records these violations as protocol errors and categorize these errors. You can view these protocol errors in the Status tab of the External Protocol Analyzer Setup dialog box in the Logic Analyzer GUI.

You can configure received frame level checks in a data capture setup using the Capture Options tab of the External Protocol Analyzer Setup dialog box in the Logic Analyzer GUI.

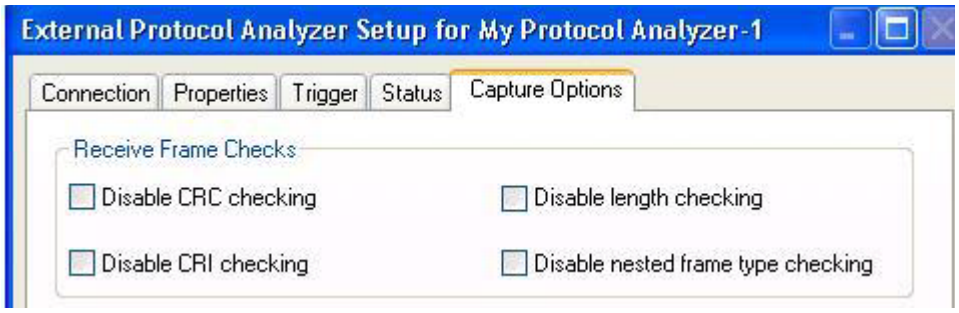
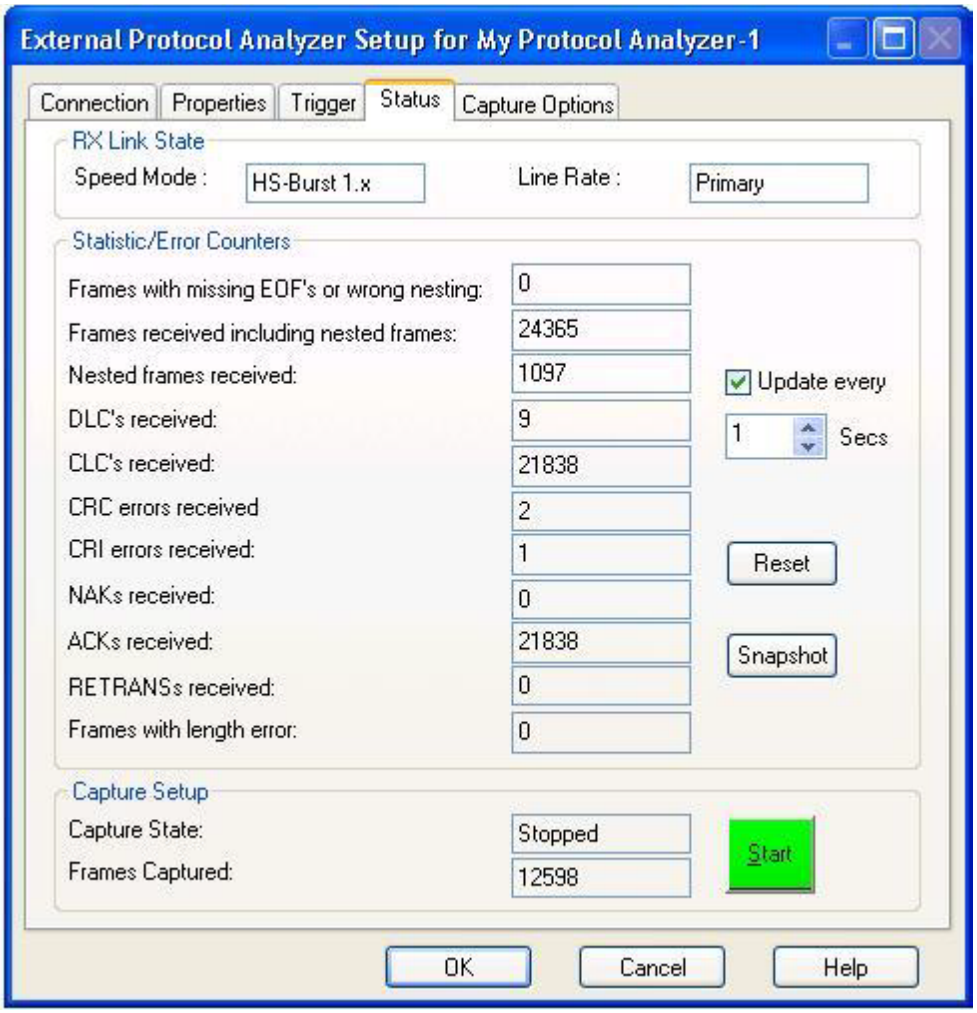


Figure 25 Receive frame checks in capture

On enabling these checks, the frames captured using either DigRF Exerciser or Analyzer module are checked for the selected protocol errors and the error statistics for the captured data is displayed as follows in the Status tab.



To know how to configure data capture setup and view the capture statistics, refer to the topic, **Configuring a Tx or Rx Data Capture Setup** and **Starting the Data Capture**.

Analyzing the Captured DigRF Data

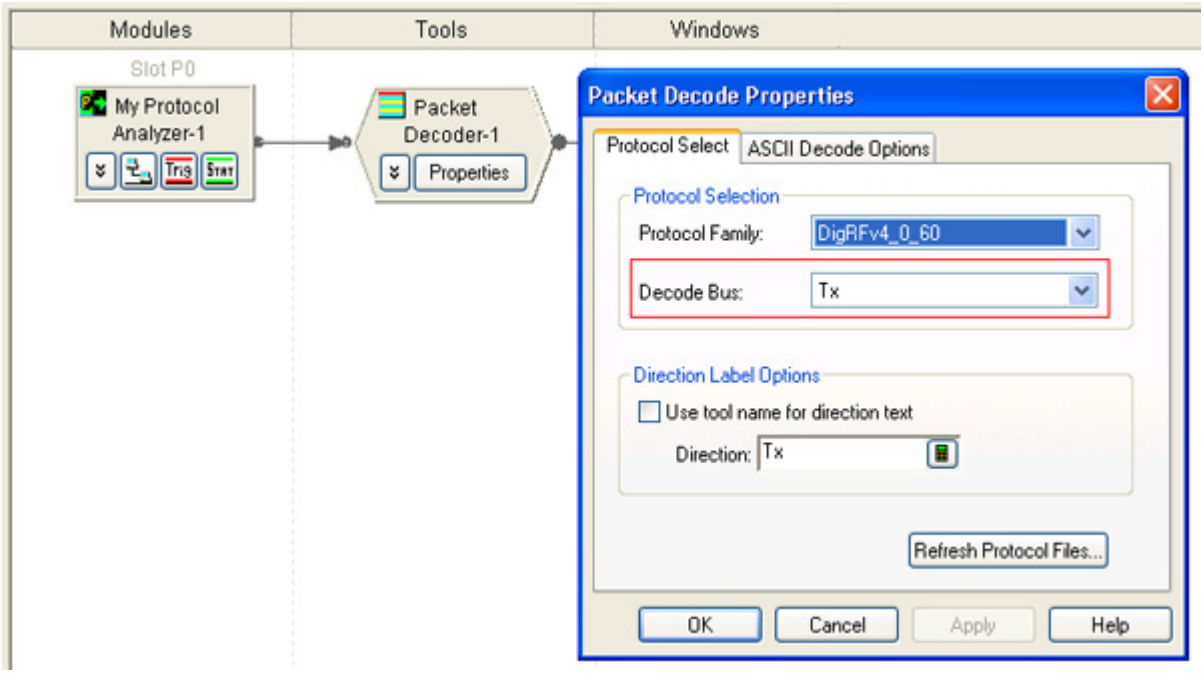
Introduction to DigRF Analysis Tools

Once you have captured DigRF data using either DigRF Exerciser or Analyzer module and obtained this data in the Logic Analyzer application through a session, you can view, decode, interpret, and analyze this captured data. You do this using various DigRF analysis tools. These tools are installed while installing RDX test platform and are available in the Logic Analyzer GUI. Some tools that help you in cross domain signal testing and analysis are not installed as a part of the RDX test platform but these tools interoperate with RDX test platform on installation. This topic introduces you to the tools that are either part of RDX test platform or interoperate with RDX test platform to help you analyze data in digital or RF domain.

NOTE To get a detailed description of each of these tools, refer to the online help provided with each of these tools.

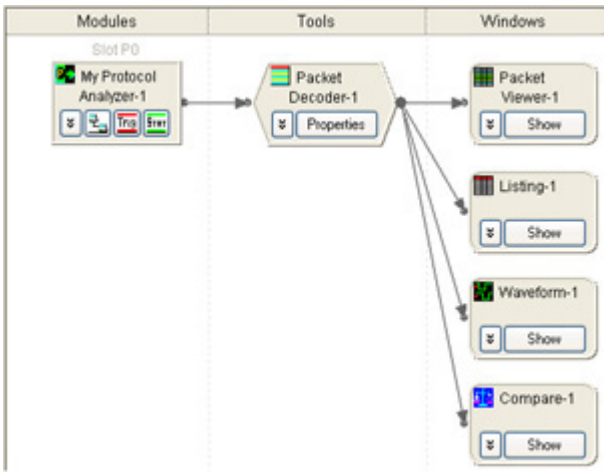
Packet Decoder (Decoding DigRF Packets)

Packet Decoder interprets the captured DigRF packets and presents an easy to understand description of the packets in viewing tools such as Packet Viewer in the Logic Analyzer GUI. While using the Packet Decoder tool, ensure that you select the appropriate protocol and the decode bus matching the packets that you want the Packet Decoder to decode. Else, it will not displays accurate results.



You can view the packets decoded by Packet Decoder as:

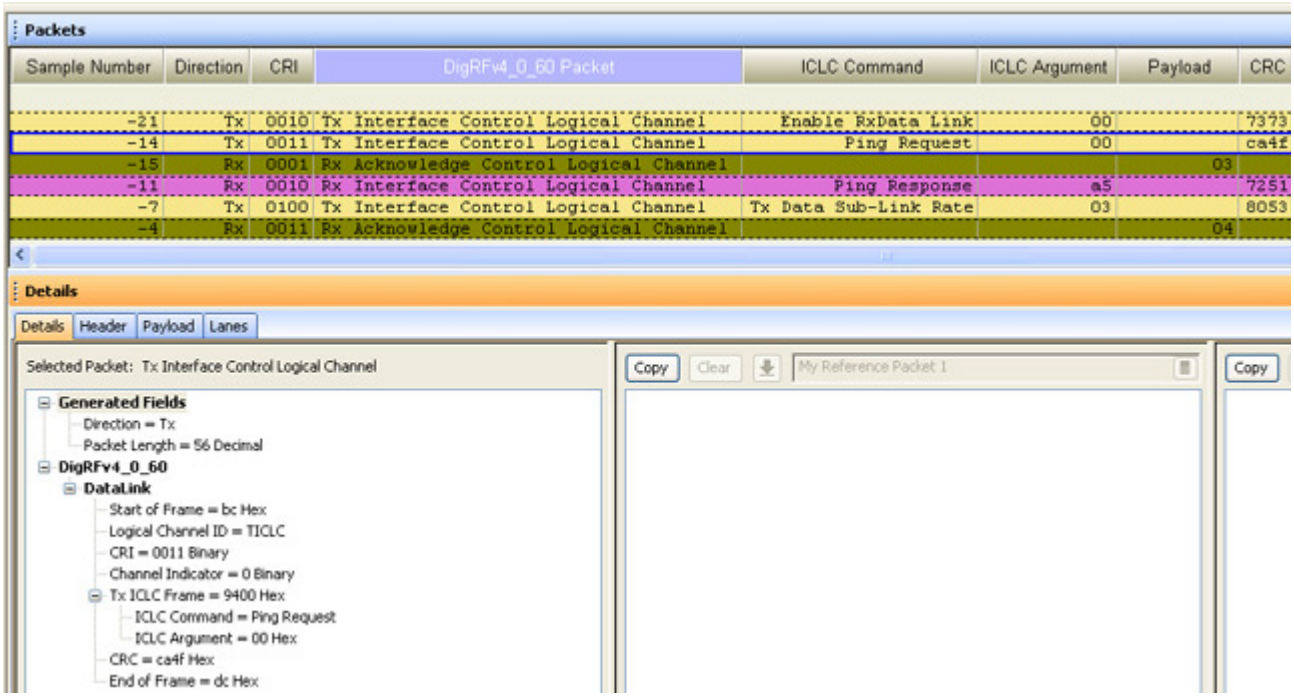
- Decoded packets in Packet Viewer
- Waveforms in Waveform Viewer
- Listing
- Compare Display (comparing data from different acquisitions)



Packet Viewer (Viewing DigRF Packets)

The Packet Viewer tool displays the DigRF packets decoded by Packet Decoder. The Packer Viewer window is customized for the protocol family being decoded. For a DigRF packet, it displays the frame components such as Header, Payload, CRC, CRI, EOF/EOT, and length of the frame. Using this tool, you can also perform DigRF packet comparison and debugging.

If you have configured dual capture, you can view the co-related Tx and Rx packets exchanged between BBIC and RFIC using the Packet Viewer tool. The following screen displays such a sequence of packets. All the packets are displayed with a timestamp.



Signal Extractor (Extracting DigRF IQ Data)

Signal Extractor is a utility in the logic analyzer framework that allows extracting the IQ data from the DigRF data packets using a specific set of DigRF commands/algorithms. You can view this extracted IQ data in either the Waveform Viewer, as a Listing, or send it to the Agilent VSA software for further RF analysis.

While extraction, it only extracts the IQ data from DigRF data frames and excludes protocol data and DigRF control frames from extraction.

You can use the Signal Extractor tool in Logic Analyzer GUI if you have the appropriate license for this tool. However, a license is not needed if a connection has been established with the DigRF Exerciser/Analyzer module used for data capture.

NOTE

A new set of APIs have been provided in RDX test platform Release 1.9. It is possible to extract the IQ data directly using the newly added APIs instead of using the Signal Extractor tool in the Logic Analyzer GUI. The direct IQ data extraction is much faster than using the Signal Extractor tool. Based on the parameters that you specify for IQ data extraction, the new APIs fetch the required number of frames and extract the IQ data from these frames. You can save the extracted IQ data in a CSV file and use this file for further signal analysis in VSA. Refer to the API help to know more about the new APIs.

The direct IQ data extraction using the new set of APIs is licensed. You need to have the appropriate hardware license to use these new APIs.

Waveform Viewer

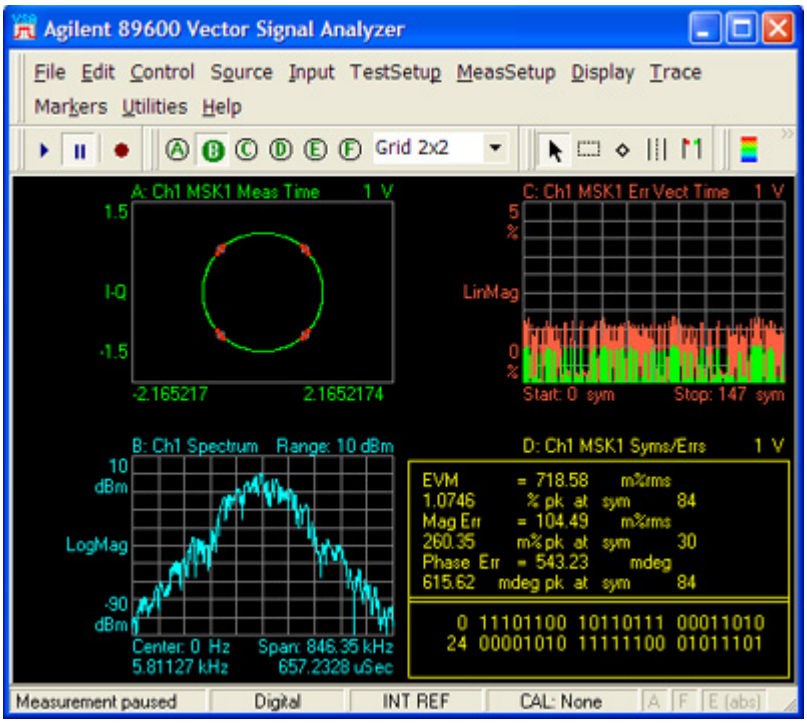
The Waveform Viewer displays the IQ data extracted from the DigRF packets in a D-to-A view.

VSA (Sending data to VSA for further Analysis)

Agilent's Vector Signal Analysis software (VSA) allows RF analysis of the IQ waveform data. It is available as a standalone product and needs to be installed separately from the RDX test platform. Once installed, you can send the extracted IQ data from Signal Extractor to VSA using the VSA GUI, which connects it to Signal Extractor.

VSA measures carrier offset, Error Vector Magnitude (EVM) and frequency error for QPSK, QAM, GSM, EDGE, WiMAX, and W-CDMA etc.

VSA lets you analyze signals and gather the data to troubleshoot signal problems.



To know more about how to use VSA in performing RF analysis of captured data, refer to the topics Configuring Data Capture with VSA Integration on page 50 and Analyzing Captured Data using VSA on page 93.

Validating a DigRF Frame Structure

You can validate if the structure of DigRF frames received from DUT (RFIC or BBIC) is as per the DigRF specifications.

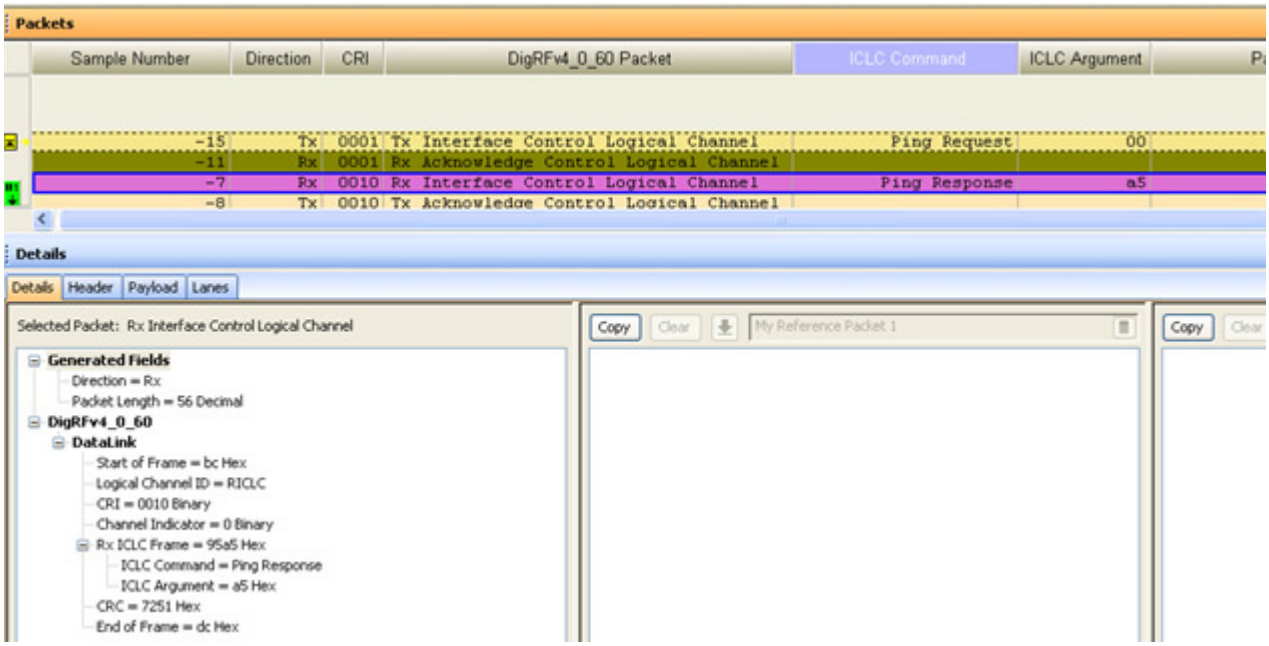
To accomplish this, you can capture the frames received from DUT using the DigRF Exerciser or Analyzer module and view the captured frames in Packet Viewer and Packet Decoder to validate and analyze the structure.

You can check if the frame components such as SOF, Header, Payload, CRC, EOF/EOT and length in a frame are as per the specifications. You can also validate the structure of specific types of frames such as nested frames or SYS-BURST (low speed) data frames to see if the construction of such frames is as per the specifications.

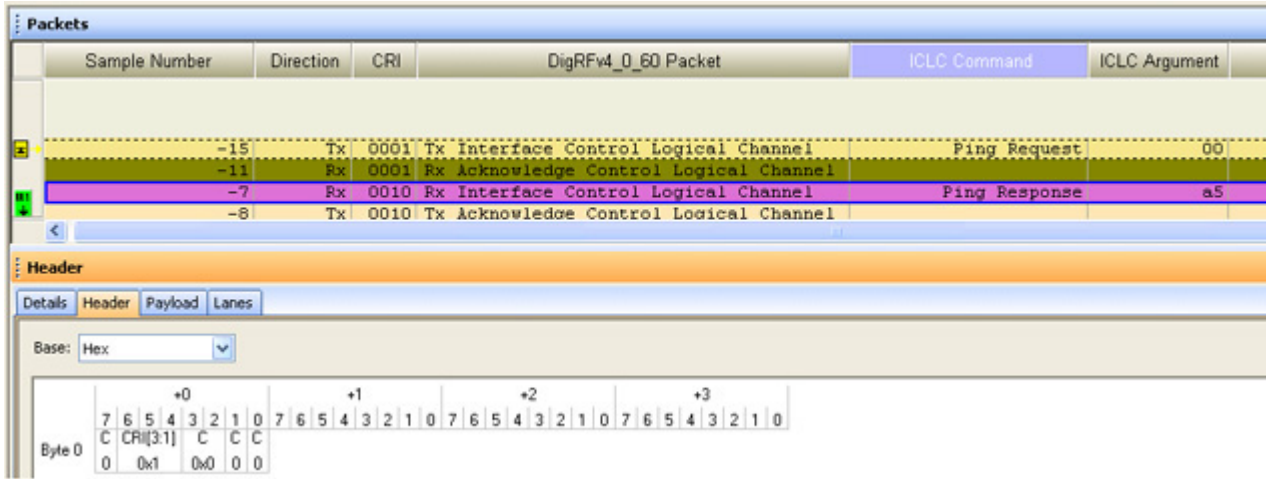
In this topic, some examples are included to display the details and structure of specific DigRF frames that have been captured using DigRF Exerciser module and displayed in Packet Viewer. In these examples, stimulus is provided using DigRF Exerciser and then dual capture is done to validate the received frames.

Example 1 - Validating a Control Frame Structure

In this example, DigRF Exerciser emulates a BBIC and sends a Ping Request control frame as stimulus to DUT (RFIC). The Tx and Rx data is captured using DigRF Exerciser, decoded using Packet Decoder, and decoded packets are displayed in Packet Viewer. In the following screen, the details of the Ping Response frame received from RFIC are displayed in Packet Viewer.

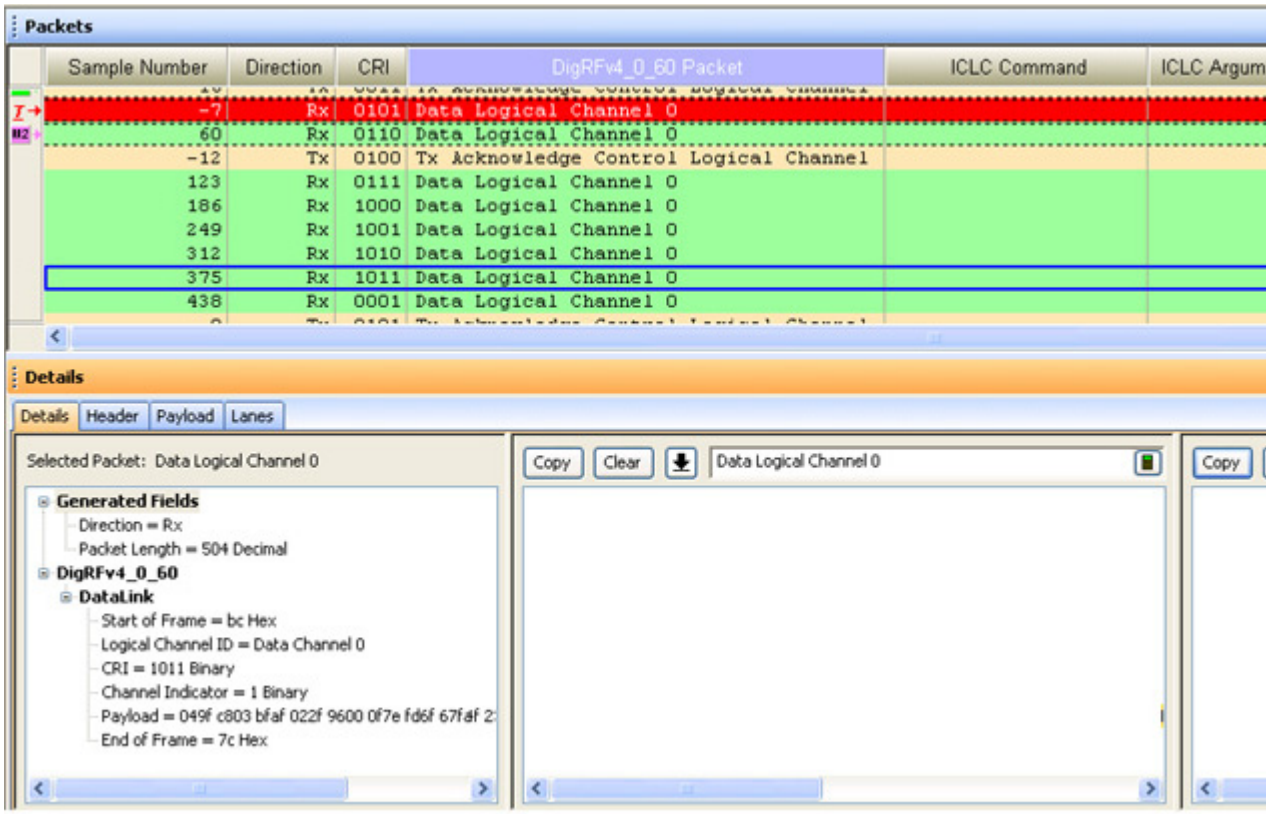


The following screen displays the header of the Ping Response frame received from RFIC.



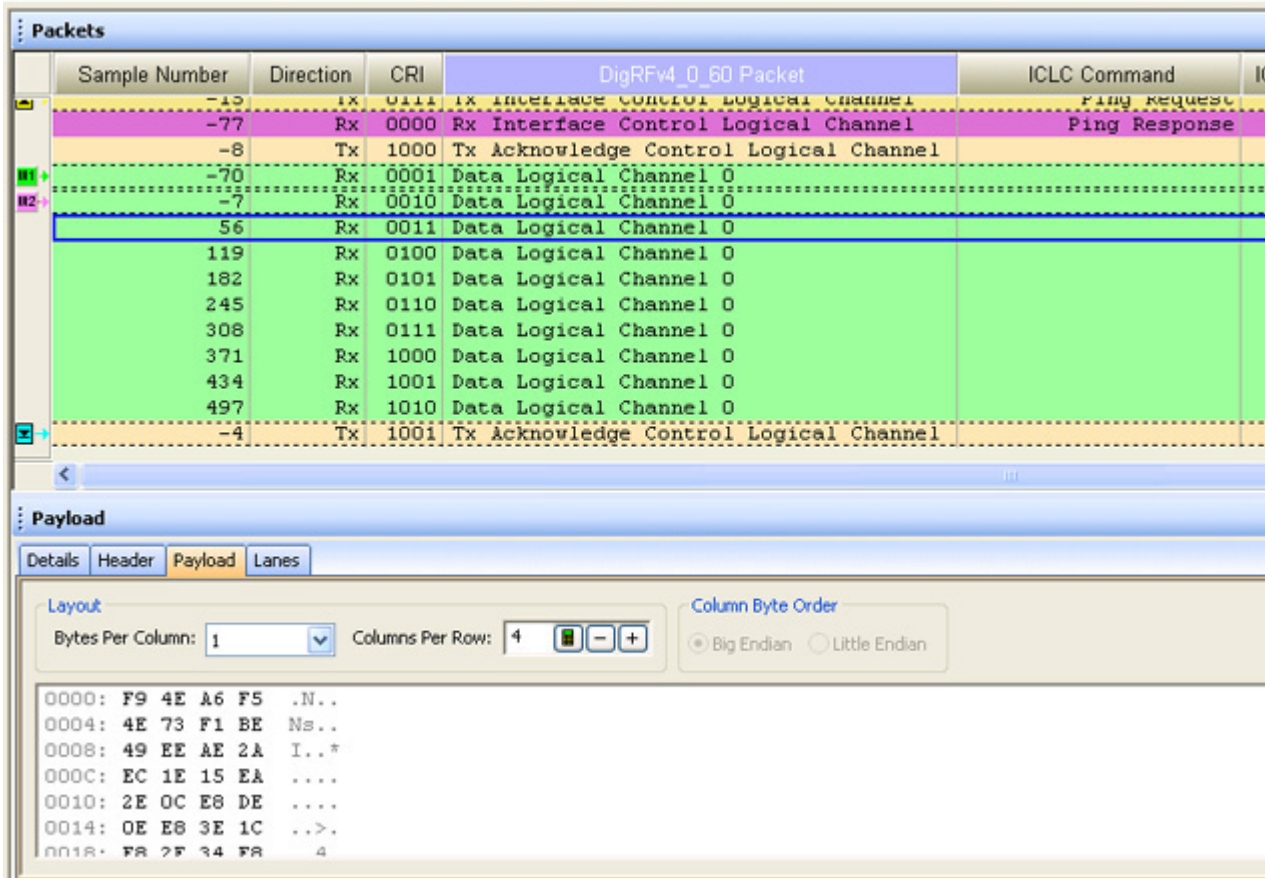
Example 2 - Validating a Retransmitted Frame Structure

The following screen displays a retransmitted frame captured using DigRF Exerciser and displayed in Packet Viewer. The header and other details of the retransmitted frame are displayed in the lower pane of the Packet Viewer.



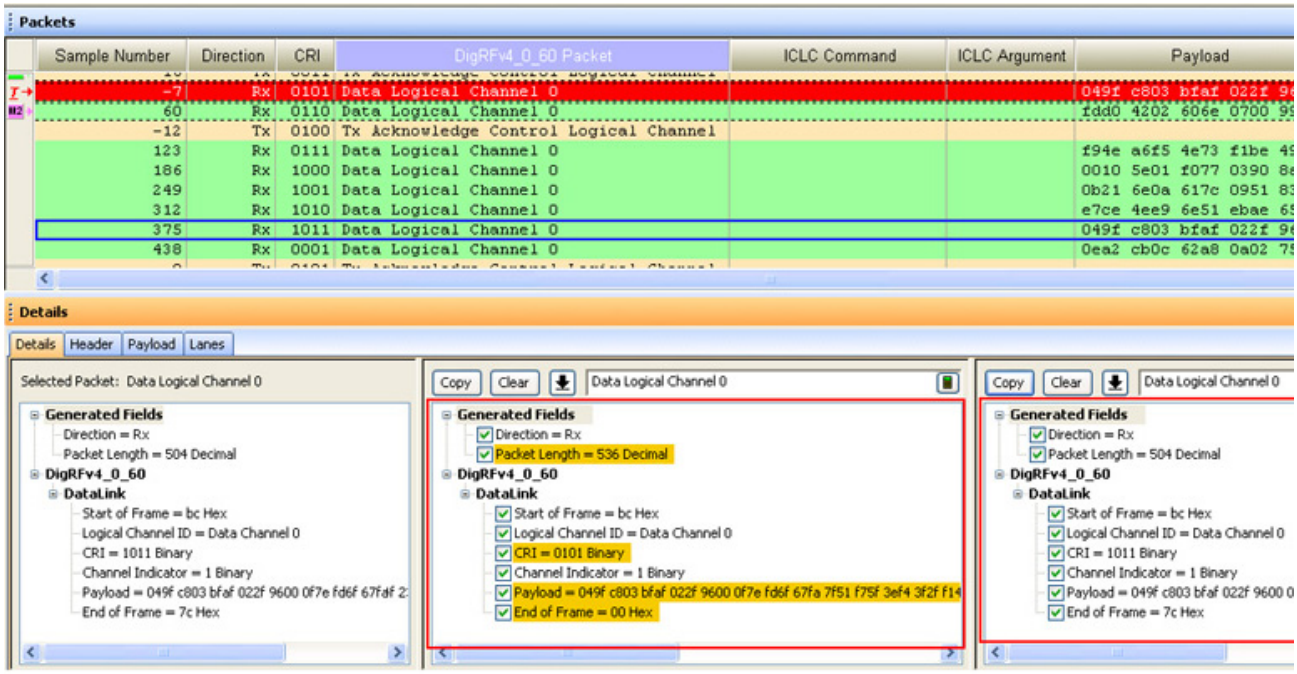
Example 4 - Validating a High Speed Data Frame Structure

The following screen displays a burst of LTE Rx data frames received from an RFIC in the HS-BURST mode. The payload of one of these data frames in the burst is also displayed in the lower pane of the Packet Viewer.



Example 5 - Comparing the Structure of Frames

In the following example, the structure of two data frames received from an RFIC is compared in Packet Viewer. The frames are selected from the list and copied in the highlighted sections by clicking the Copy button. The first frame structure is of a data frame with framing error in the end of frame. The second frame structure is of the data frame retransmitted in response to the NACK received for the first frame. The differences in the structure of the two frames are highlighted by Packet Viewer.


Packets
Sample Number
Direction
CRI
DigRFv4_0_60 Packet
ICLC Command
ICLC Argument
Payload
-7 Rx 0101 Data Logical Channel 0 049f c803 bfaf 022f 9
60 Rx 0110 Data Logical Channel 0 fdd0 4202 606e 0700 9
-12 Tx 0100 Tx Acknowledge Control Logical Channel
123 Rx 0111 Data Logical Channel 0 f94e a6f5 4e73 f1be 4
186 Rx 1000 Data Logical Channel 0 0010 5e01 f077 0390 8
249 Rx 1001 Data Logical Channel 0 0b21 6e0a 617c 0951 8
312 Rx 1010 Data Logical Channel 0 e7ce 4ee9 6e51 ebae 6
375 Rx 1011 Data Logical Channel 0 049f c803 bfaf 022f 9
438 Rx 0001 Data Logical Channel 0 0ea2 cb0c 62a8 0a02 7
Details
Details
Header
Payload
Lanes
Selected Packet: Data Logical Channel 0
Generated Fields
Direction = Rx
Packet Length = 504 Decimal
DigRFv4_0_60
DataLink
Start of Frame = bc Hex
Logical Channel ID = Data Channel 0
CRI = 1011 Binary
Channel Indicator = 1 Binary
Payload = 049f c803 bfaf 022f 9600 0f7e fd6f 67faf 2
End of Frame = 7c Hex
Copy
Clear
Data Logical Channel 0
Generated Fields
Direction = Rx
Packet Length = 536 Decimal
DigRFv4_0_60
DataLink
Start of Frame = bc Hex
Logical Channel ID = Data Channel 0
CRI = 0101 Binary
Channel Indicator = 1 Binary
Payload = 049f c803 bfaf 022f 9600 0f7e fd6f 67fa 7f51 f75f 3ef4 3f2f f14
End of Frame = 00 Hex
Copy
Clear
Data Logical Channel 0
Generated Fields
Direction = Rx
Packet Length = 504 Decimal
DigRFv4_0_60
DataLink
Start of Frame = bc Hex
Logical Channel ID = Data Channel 0
CRI = 1011 Binary
Channel Indicator = 1 Binary
Payload = 049f c803 bfaf 022f 9600 0
End of Frame = 7c Hex

Analyzing Captured Data using VSA

This topic describes how you can send the DigRF data captured using the DigRF Exerciser/Analyzer module to VSA for further RF signal analysis.

You can perform offline or online analysis of data using VSA. This topic describes both these modes of data analysis using VSA.

Offline analysis of captured data using VSA

Offline analysis here means that a connection is not required with the DigRF Exerciser/Analyzer hardware while performing data analysis in VSA. In this mode, you can save the data captured using the DigRF Exerciser/Analyzer module in a file using the Logic Analyzer GUI. You can later view, analyze, and send this saved data from this file to the VSA GUI for offline analysis.

In offline analysis, when VSA reaches the end of the Logic Analyzer data capture, it returns to the beginning of the data and continues the measurement. In this analysis, VSA can only fetch already captured data from Logic Analyzer and runs this captured data repeatedly. It cannot trigger the Logic Analyzer for recapture.

To perform offline analysis using VSA:

1 In the Logic Analyzer GUI, save the data that you captured using the DigRF Exerciser/Analyzer module. Refer to the topic Viewing the Captured Data Offline on page 65 to know how to save the captured data.

2 In the Logic Analyzer GUI, import the captured data from the file for offline viewing and analysis. Refer to the topic Viewing the Captured Data Offline on page 65 to know how to import the saved data.

3 Add the **Signal Extractor** tool with the imported data module in the Logic Analyzer GUI. This tool extracts IQ data from the captured data and sends it to the VSA GUI for RF analysis. VSA can input data from selected Logic Analyzer software tools. The first supported tool is the Signal Extractor. The VSA will only take data from software tools that receive their input from hardware modules. The VSA will not receive data from a tool whose input is another tool's output. In offline mode, when no connection with the DigRF Exerciser/Analyzer hardware is there, you need an appropriate license to use the Signal Extractor tool.

4 Start the VSA GUI.

5 Link the VSA GUI to the Logic Analyzer application.

   a VSA gets the Logic Analyzer address using the 89600 IO Connections software utility.

   b The 89600 IO Connections software utility is installed with the VSA software and is located at **Start** > (All) **Programs** > **Agilent 89600 VSA** > **Logic Analyzer** > **IO Connections**. If the Logic Analyzer application resides on the same PC as the VSA, then use the name "localhost."

   c In the VSA GUI, click **Utilities** > **Hardware** > **ADC** 1. **Clear Simulate Hardware** if currently selected and select **Agilent VSA Logic Analyzer Input**. VSA will then link to the Logic Analyzer application.

6 Analyze the saved data offline in the VSA GUI.

Online analysis of captured data using VSA

Online analysis here means that the Logic Analyzer GUI is connected to the DigRF Exerciser/Analyzer hardware for data capture and the captured data is simultaneously sent from Logic Analyzer to VSA for analysis while being connected to the DigRF Exerciser/Analyzer hardware. In this type of analysis, VSA can generate real time graphs from the captured data received from the Logic Analyzer GUI.

In online analysis, VSA runs to the end of the current Logic Analyzer data capture buffer and instructs or triggers the Logic Analyzer to run again for recapture.

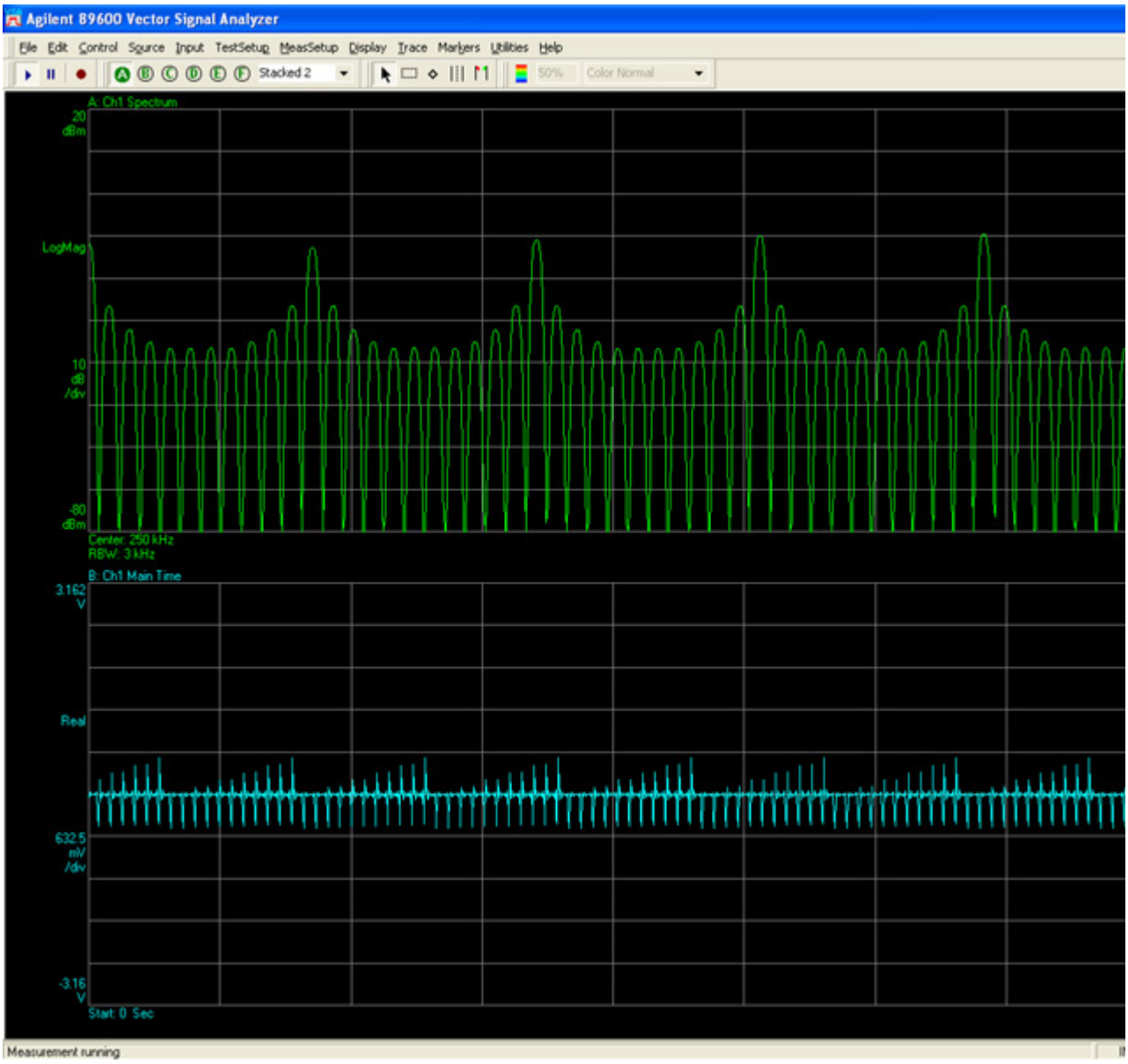
For online analysis of data in VSA, some configurations are required for VSA integration with the Logic Analyzer GUI. To know about these configurations on the Logic Analyzer GUI and the VSA GUI, refer to the topic Configuring Data Capture with VSA Integration on page 50.

Once you have performed these configurations, add a Signal Extractor tool to extract IQ data from the captured data and to send it to VSA for analysis. VSA can take data from selected Logic Analyzer software tools. The first supported tool is the Signal Extractor. VSA takes data from software tools that receive their input from hardware modules. VSA does not receive data from a tool whose input is another tool's output.

The captured data is available in real time for analysis in VSA when you click the  toolbar button in the Logic Analyzer GUI and the  toolbar button in VSA GUI. On

clicking these buttons, the data capture gets started, the captured data is uploaded in Logic Analyzer GUI, and the extracted IQ data using Signal Extractor is passed to VSA for online RF analysis.

The following screen displays the extracted IQ data passed from Signal Extractor to VSA for online analysis.



3
Cross Domain Testing of an RFIC

RDX test platform provides tools to perform cross domain testing of an RFIC covering the DigRF as well as RF sides of an RFIC to achieve a complete testing scenario for the RFIC.

You can aim at testing whether the data received by RFIC over the DigRF link passes correctly to the wireless side of RFIC and vice versa. Another goal of such testing can be testing the quality of the modulation.

RDX test platform helps you perform cross domain RF and digital testing by providing stimulus, capture, and analysis tools in RF and digital domains. Some of these tools are a part of RDX test platform and some interoperate with RDX test platform to provide an environment for complete testing. This topic describes how you can do cross domain testing using these tools. To get a detailed description of each of these tools, refer to the online help provided with each of these tools. This topic only focuses on how you can use these tools together to perform cross domain testing.

For cross domain testing using RDX test platform, you can use the tools as follows:

- **DigRF stimulus** - Use the DigRF Exerciser module to provide DigRF stimulus to RFIC.
- **RF stimulus** - Use the Signal Studio environment to provide RF stimulus to RFIC. You need to install Signal Studio separately as it is not installed as a part of RDX test platform. Agilent Signal Studio is a standards-based signal-creation tool that you can use for signal simulation. You can use this tool to generate reference signals to characterize and evaluate an RFIC by providing appropriate RF stimulus. Signal Studio works with the RDX test platform and supports a variety of cellular and wireless formats including WiMAX and LTE.
- **DigRF data capture** - Use either DigRF Exerciser or Analyzer module to capture (Tx, Rx, or both) DigRF data.
- **DigRF Analysis tools** - View, decode, and analyze the captured DigRF data using various DigRF Analysis tools in Logic Analyzer.

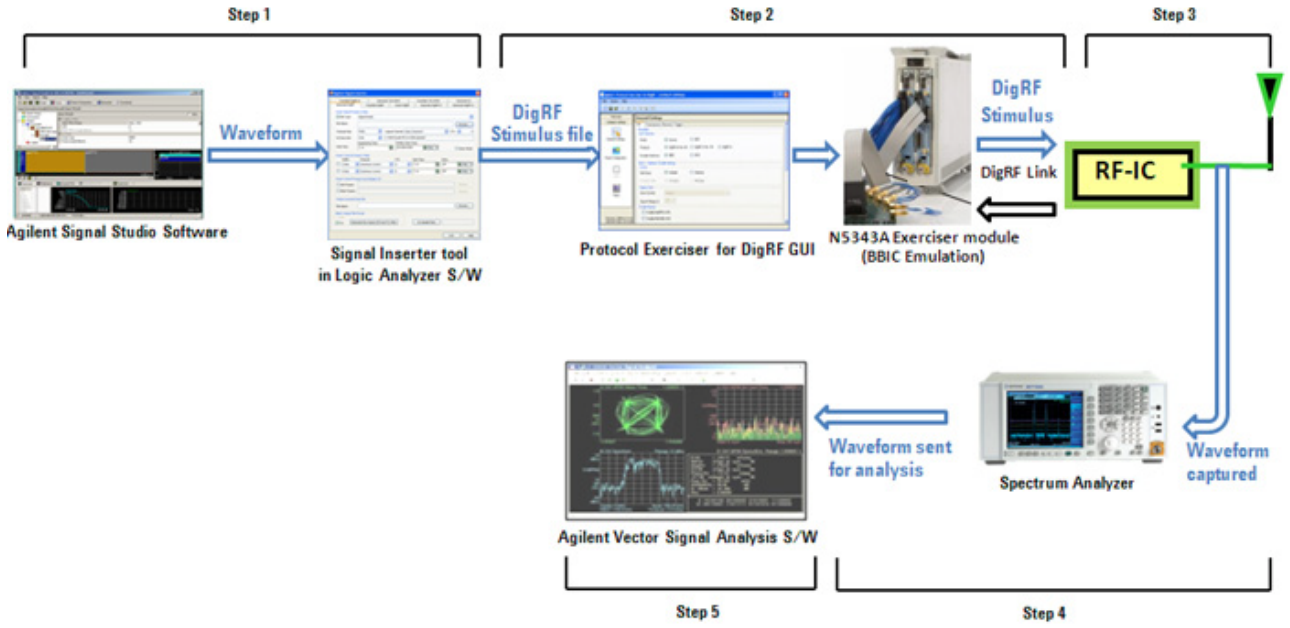
- **RF analysis** - Send the captured DigRF data after extraction to VSA environment for RF level analysis. You need to install VSA separately as it is not installed as a part of RDX test platform.

Using the above-mentioned tools, you can test the Transmit as well Receive paths of an RFIC to cover the complete testing paths. The following examples describe the transmit and receive path testing of an RFIC.

RFIC transmit path testing

The RFIC transmit path testing, in this example, aims at validating whether or not an RFIC depacketizes the DigRF frames received from BBIC over the DigRF link into IQ data and transmits successfully over the air interface. The example checks if any distortions or errors are introduced in the digital data during the depacketization and transmission from RFIC.

The following diagram illustrates this flow of testing using appropriate tools:



The following is the explanation of the flow of RFIC testing with reference to the above diagram:

1 Create DigRF Stimulus for RFIC - In step 1, a waveform is created using Agilent Signal Studio software. This

waveform is then packetized into DigRF packets in a DigRF stimulus file using the Signal Inserter tool.

2 Provide DigRF stimulus to stimulate the RFIC - In step 2, DigRF Exerciser emulates a BBIC over a DigRF link configured between DigRF Exerciser and RFIC (DUT). The stimulus file created in step 1 is imported in the DigRF Exerciser GUI to get the DigRF frames. The DigRF frames are then transmitted to RFIC on the TxData sublink.

3 In step 3, RFIC depacketizes the stimulus, converts digital signals into analog and generates RF waveform and transmits it over the air interface.

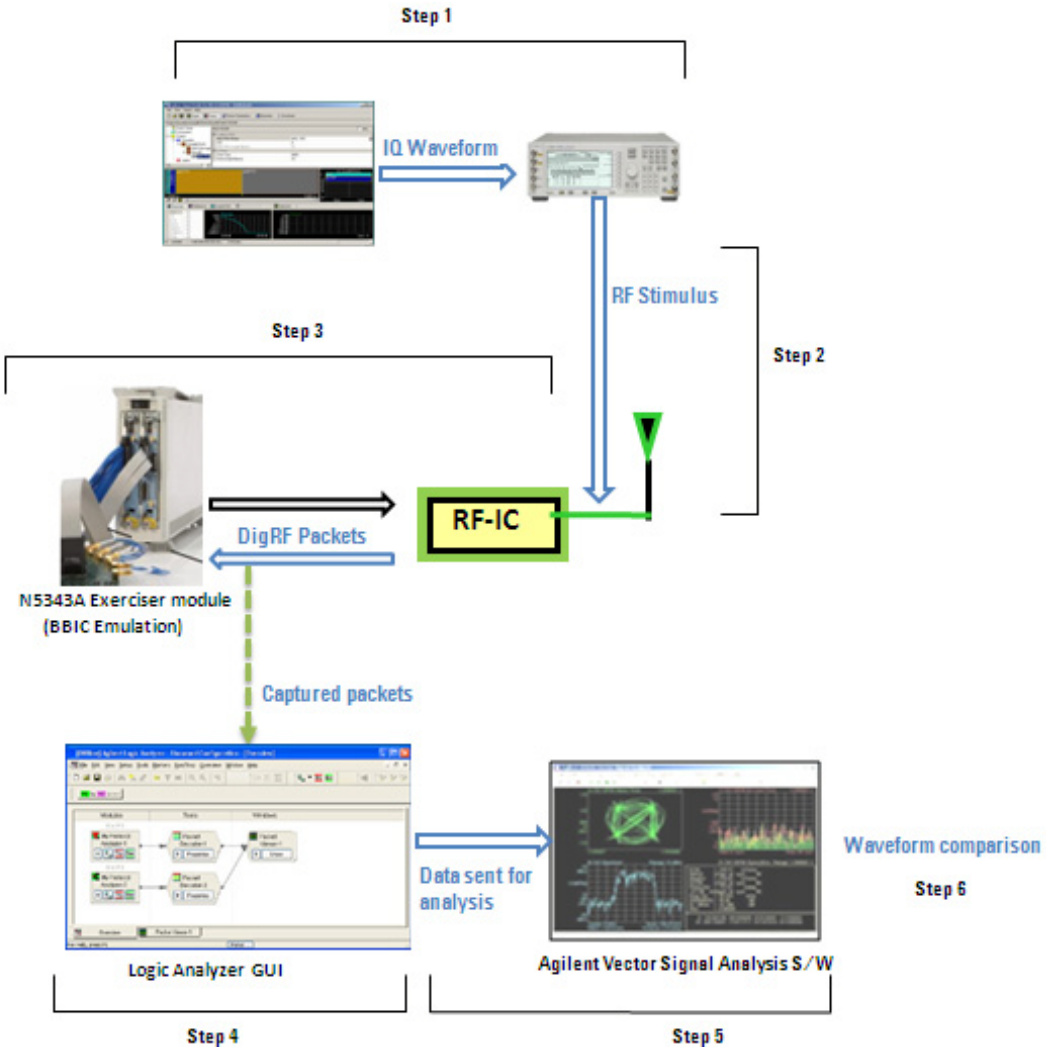
4 In step 4, Agilent Spectrum Analyzer captures the transmitted waveform from the antenna side and the captured waveform is sent to Agilent Vector Signal Analyzer (VSA).

5 In step 5, the waveform used in step 1 is compared with the waveform generated in step 4 to check if there are any distortions or glitches in the data during the overall transmission sequence.

RFIC receive path testing

The RFIC receive path testing in this example aims at validating whether or not an RFIC digitizes the signals received from the air interface into digitized IQ data and transmits successfully over the DigRF link as DigRF frames. The example checks if any distortions or errors are introduced in the data during the packetization and transmission from RFIC over the DigRF link.

The following diagram illustrates this flow of testing using appropriate tools:



The following is the explanation of the flow of RFIC testing with reference to the above diagram:

1. Create RF Stimulus for RFIC - In step 1, a waveform is created using Agilent Signal Studio software. This waveform is then modulated and an analog waveform is generated using Agilent Vector Signal Generator software.
2. Provide RF stimulus to stimulate RFIC - In step 2, Agilent Vector Signal Generator software sends the RF stimulus created in step 1 to RFIC.
3. In step 3, RFIC processes the RF stimulus, renders the digital IQ, packetizes it, and transmit it as DigRF packets over the DigRF link to a BBIC or the DigRF Exerciser emulating a BBIC.

4 In step 4, DigRF Exerciser or Analyzer module is used to capture the DigRF packets that RFIC sent in step 3. Captured packets are obtained in the Logic Analyzer GUI.

5 In step 5, the captured data is further sent to Agilent Vector Signal Analyzer (VSA) software to analyze the captured data. VSA regenerates the waveform from the captured data.

6 The waveform used in step 1 is compared with the waveform generated in step 5 to check if there are any distortions or glitches in the data during the overall sequence of transmission.

4 Testing BBIC and RFIC Integration

This topic provides an example to describe how you can test the integrated RFIC and BBIC by monitoring and analyzing the data exchanged between these over the DigRF link.

To test the RFIC and BBIC integration scenario, you can use the DigRF Analyzer module that provides non intrusive monitoring and capturing of the DigRF traffic between the RFIC and BBIC. Using this module, you can capture the data transmitted on the TxData sublink (BBIC to RFIC) as well as the data transmitted on the RxData sublink (RFIC to BBIC).

You can also set up trigger conditions to ensure that the DigRF Analyzer module starts the data capture when the trigger condition is met.

The following sections describe how to configure capture settings to use DigRF Analyzer to capture data exchanged both ways over the DigRF link. Before configuring these capture settings, ensure that the hardware configurations are complete for this setup.

- The chassis having the DigRF Analyzer module must connect to the system controller hosting the RDX software.
- The DigRF Analyzer module must connect to the target test system (DUT with BBIC and RFIC) through a Flying Leads or a Soft Touch probe.
- RFIC and BBIC are integrated.

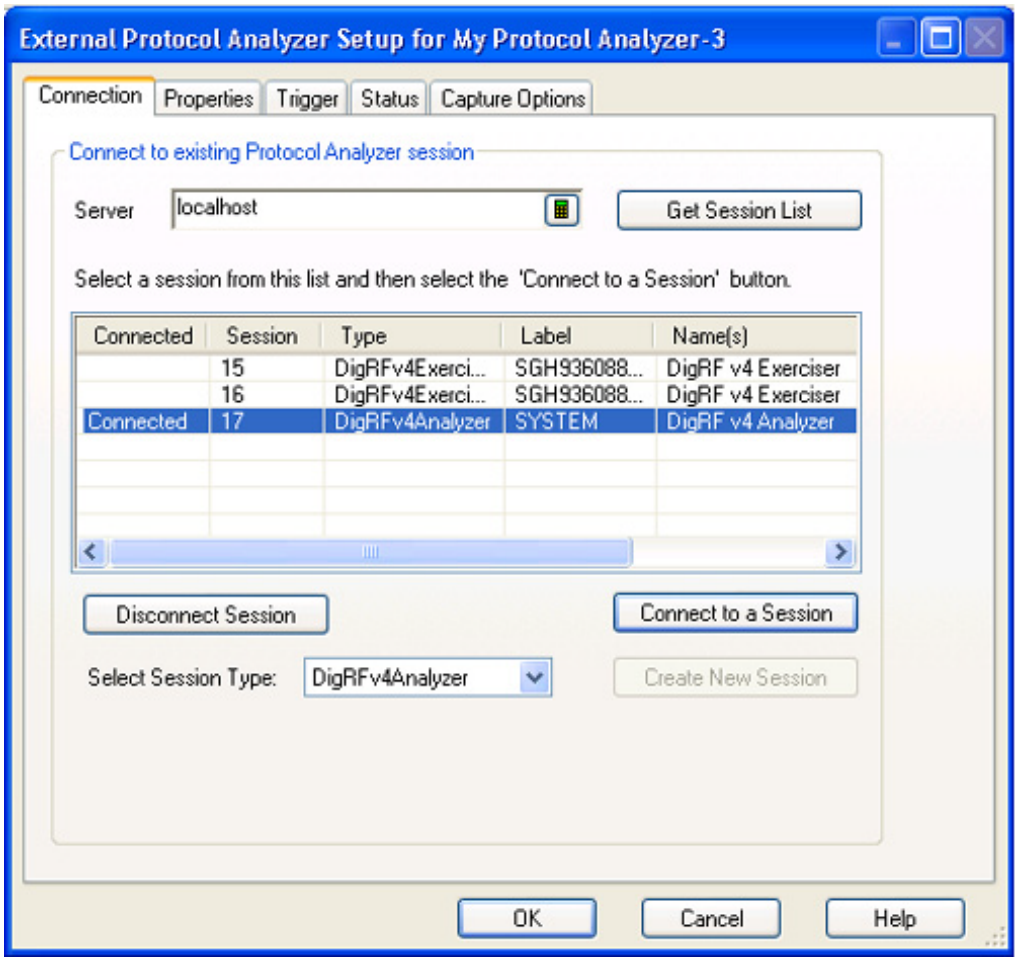
NOTE In the screenshots used in this topic, DigRF Exerciser modules are used in place of a BBIC and an RFIC to emulate these two ICs. The DigRF data exchanged between these two Exerciser modules is captured to demonstrate the RFIC and BBIC integration testing scenario.

Creating a session with DigRF Analyzer module

You use the Logic Analyzer GUI to control, configure, and use the data capture capabilities of DigRF Analyzer module. Therefore, a session is needed with the DigRF Analyzer

module to establish a connection between the Logic Analyzer GUI hosted on the system controller and the DigRF Analyzer module in the chassis.

The following screen displays a new session created to connect to the DigRF Analyzer module. To know more about sessions, refer to the topicEstablishing a Connection with DigRF Exerciser/Analyzer Module on page 33.

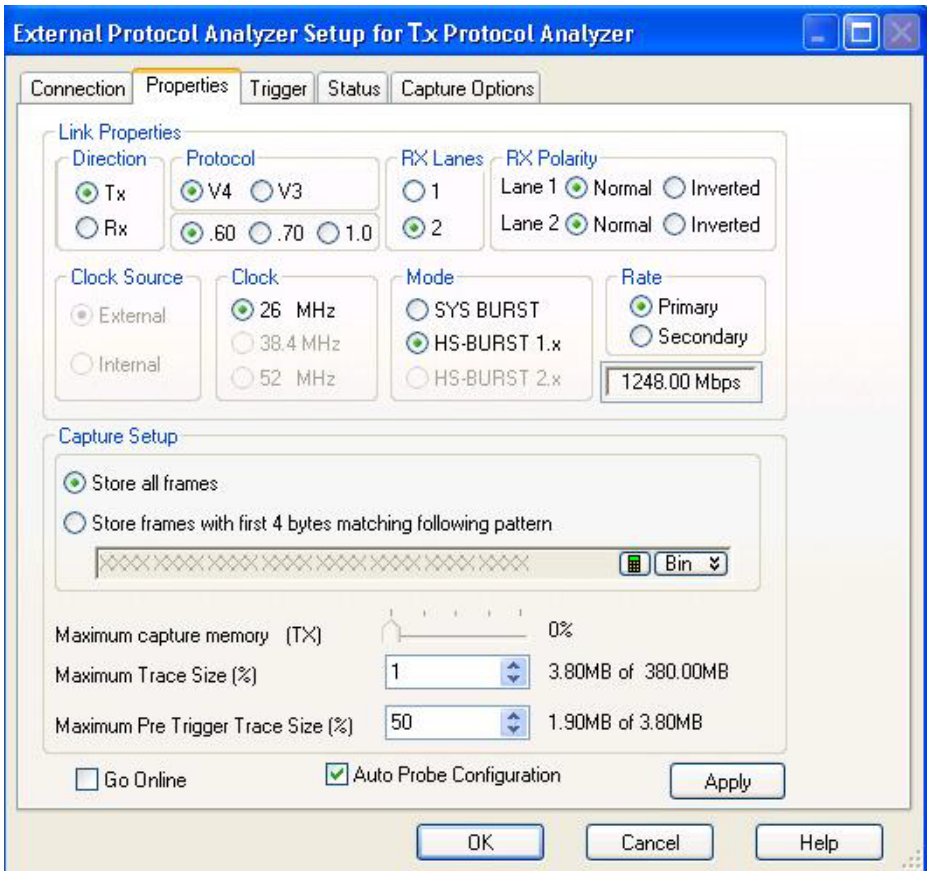


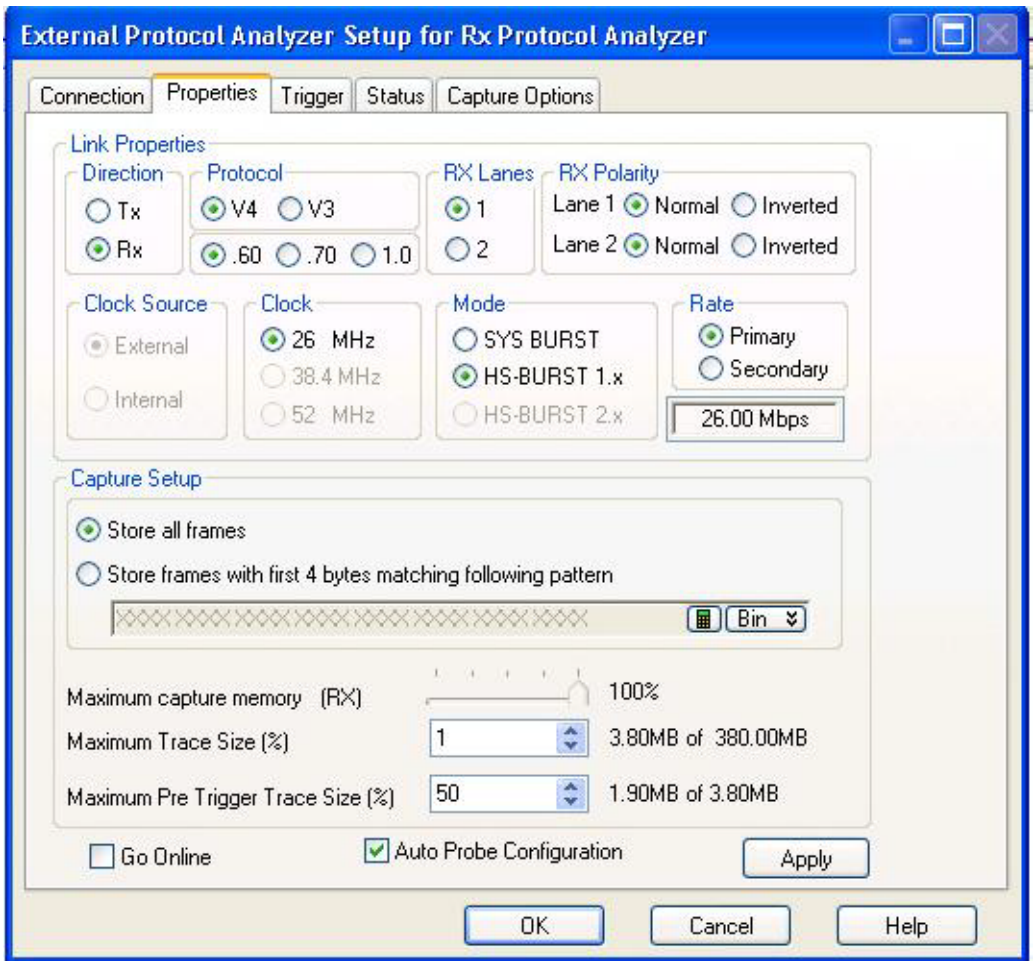
After a connection is created, more tabs have been added in the above dialog box to configure the data capture settings and start the data capture. Using the same session, another instance of the External Protocol Analyzer setup is created in Logic Analyzer GUI. One setup will be used for Tx and another for Rx data capture.

Creating Tx and Rx Data Capture Setups

To capture the Tx and Rx DigRF data, you need to specify data capture settings separately for the Tx and Rx sides of the DigRF link. Based on these settings, DigRF Analyzer captures the data on the TxData and RxData sublinks. To know more, refer to the topic, Configuring a Tx or Rx Data Capture Setup on page 36.

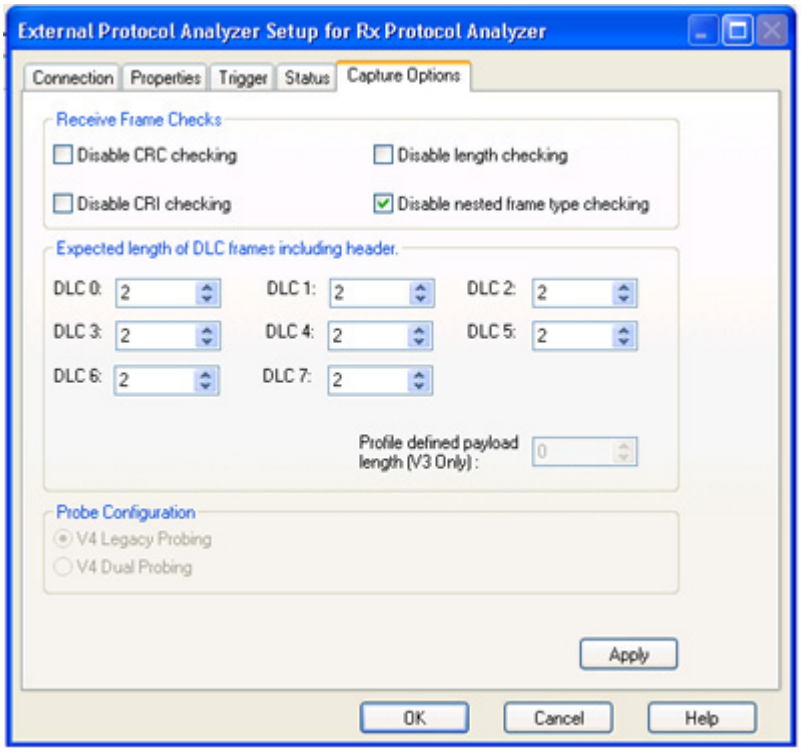
The following screens display the data capture setups for the TxData (Tx link direction) and RxData (Rx link direction) sublinks.





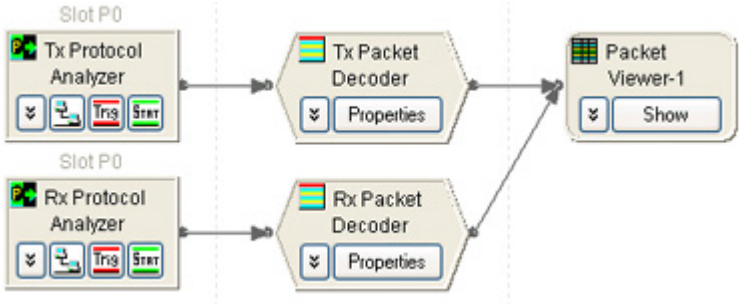
Setting up Protocol Error Checks on the Captured Data

You can select the protocol error checks to be performed on the captured data. The following screen displays the capture options set to enable CRI, CRC, and length checking for the captured frames. To know more, refer to the topic Configuring a Tx or Rx Data Capture Setup.



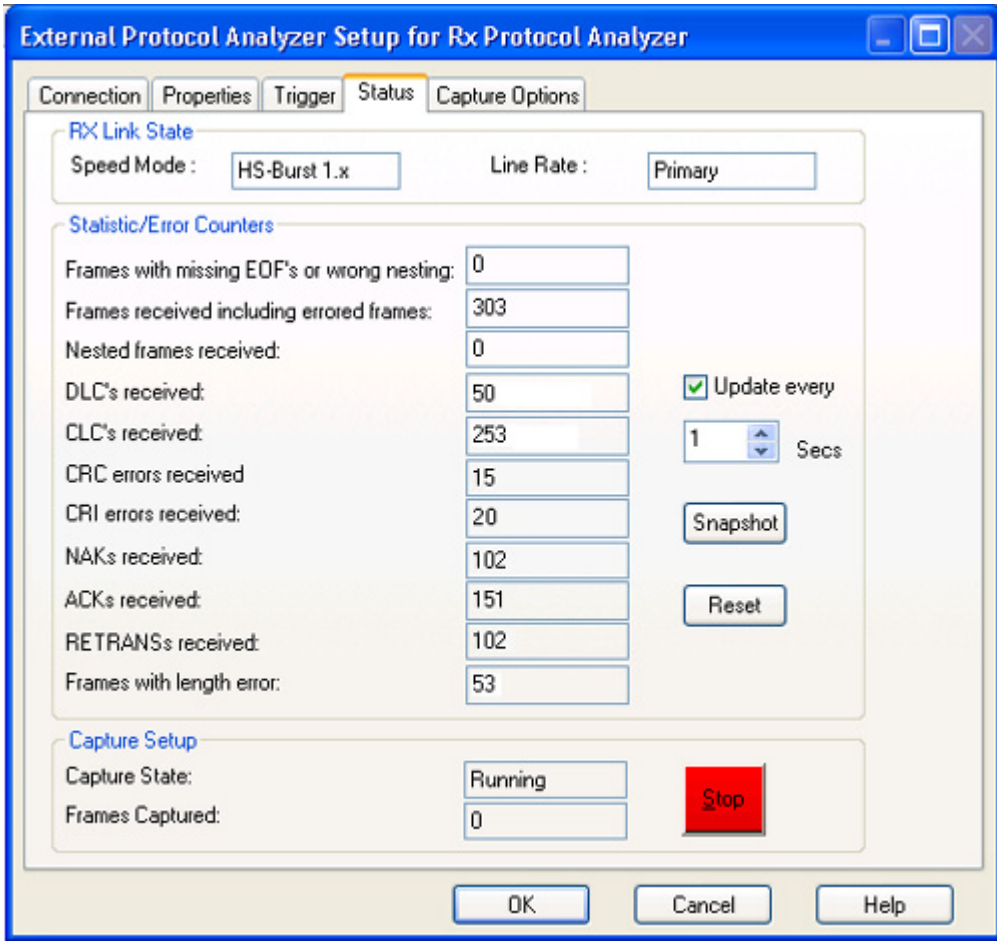
Correlating the Tx and Rx captured data

In Logic Analyzer GUI, you can either view the Tx and Rx data captured by DigRF Analyzer separately or co-relate the Tx and Rx data. Before, viewing the data, it needs to be decoded using the Packet Decoder tool. The following screen displays Packet Decoders (one with Tx and another with Rx decode bus) added to the data capture setups in Logic Analyzer GUI. To view co-related data, both the Tx and Rx Packet Decoder instances are connected to the same Packet Viewer instance.



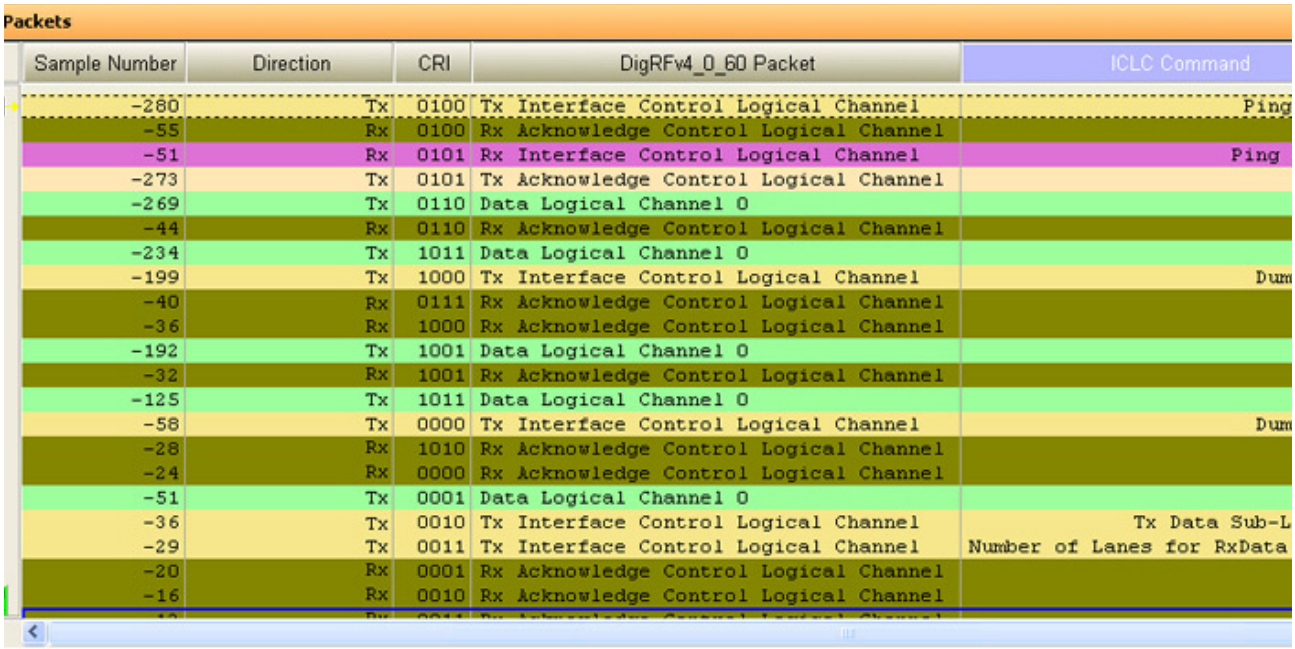
Starting the data capture

After configuring the required settings, the data capture is started in the Logic Analyzer GUI. DigRF Analyzer starts storing the captured data from the TxData and RxData sublinks in the capture memory and the statistics counters are updated. The capture statistics also displays the number of Tx and Rx frames captured with CRC, CRI, and length errors.



To know more about starting the data capture, refer to the topic Starting the Data Capture.

The captured data is then acquired into the Logic Analyzer GUI by clicking the **Run** toolbar button for display in Packet Viewer. The following screen displays the co-related data exchanged between an RFIC and BBIC.



Packets

Sample Number	Direction	CRI	DigRFv4_0_60 Packet	ICLC Command
-280	Tx	0100	Tx Interface Control Logical Channel	Ping
-55	Rx	0100	Rx Acknowledge Control Logical Channel	
-51	Rx	0101	Rx Interface Control Logical Channel	Ping
-273	Tx	0101	Tx Acknowledge Control Logical Channel	
-269	Tx	0110	Data Logical Channel 0	
-44	Rx	0110	Rx Acknowledge Control Logical Channel	
-234	Tx	1011	Data Logical Channel 0	
-199	Tx	1000	Tx Interface Control Logical Channel	Dum
-40	Rx	0111	Rx Acknowledge Control Logical Channel	
-36	Rx	1000	Rx Acknowledge Control Logical Channel	
-192	Tx	1001	Data Logical Channel 0	
-32	Rx	1001	Rx Acknowledge Control Logical Channel	
-125	Tx	1011	Data Logical Channel 0	
-58	Tx	0000	Tx Interface Control Logical Channel	Dum
-28	Rx	1010	Rx Acknowledge Control Logical Channel	
-24	Rx	0000	Rx Acknowledge Control Logical Channel	
-51	Tx	0001	Data Logical Channel 0	
-36	Tx	0010	Tx Interface Control Logical Channel	Tx Data Sub-L
-29	Tx	0011	Tx Interface Control Logical Channel	Number of Lanes for RxData
-20	Rx	0001	Rx Acknowledge Control Logical Channel	
-16	Rx	0010	Rx Acknowledge Control Logical Channel	

Extracting IQ Data from the captured data packets

You can add a Signal Extractor tool instance to the data capture setups created in the Logic Analyzer GUI to extract IQ data from the Tx or Rx data packets. The extracted data can then be viewed as a listing or a waveform.

By viewing and analyzing the co-related data from BBIC and RFIC, you can find out the root cause of the interoperability issues.

5 Troubleshooting DigRF Capture related Problems

This topic lists some of the problems that you might encounter while using the DigRF Exerciser / Analyzer modules of RDX Test platform for capturing and analyzing DigRF data.

Problem	Cause	Solution
You have configured data capture settings in Logic Analyzer and the data capture has started. However, the captured data is not displayed in the Packet Viewer instance that you have added.	• The captured data is not yet acquired from the memory of DigRF Exerciser/Analyzer module used for data capture into the Logic Analyzer GUI. Or you have not connected to a session with the DigRF Exerciser/Analyzer module while acquiring the captured data from this module. • The configurations for the Packet Decoder instance added to decode the captured packets in Logic Analyzer are not correct.	• Click the  toolbar button the Logic Analyzer GUI to acquire the captured data for display and analysis. Ensure that a session is created between the Logic Analyzer GUI and the DigRF Exerciser/Analyzer module while acquiring the data. • Check if the **Protocol Family** and **Decode bus** settings are appropriately set in the Packet Decoder instance. If you are capturing packets on the TxData sublink (BBIC to RFIC), then select Tx as the Decode bus and for packets captured over the RxData sublink, select Rx.

Problem	Cause	Solution
You have configured the stimulus and capture settings using DigRF Exerciser and stimulus results are displayed. However, the data received from DUT is not getting captured. The number of captured frames is displayed as 0 in Logic Analyzer GUI.	The capture settings might not be properly set in the Logic Analyzer GUI.	Check if the link direction configured for data capture in Logic Analyzer is correct. If you are using DigRF Exerciser for data capture: • **Tx** means data capture for Transmitter side of DigRF Exerciser • **Rx** means data capture for Receiver side of DigRF Exerciser If you are using DigRF Analyzer for data capture: • **Tx** means data capture for TxData sublink (BBIC to RFIC) • **Rx** means data capture for RxData sublink (RFIC to BBIC) Check if you have allocated DigRF Exerciser's memory for data capture. If it is left to 0%, then captured data will not be stored.
You have configured stimulus and data capture using DigRF Exerciser. The stimulus statistics is getting displayed. However, in data capture, only the data capture statistics is getting updated but the number of frames captured is displayed as 0.	The sequence in which the stimulus and capture is started is incorrect.	Start the stimulus and capture in the following sequence: 1. Start the data capture in the Logic Analyzer GUI by clicking the Start button in the Status page of the External Protocol Analyzer Setup dialog box. 2. Start the stimulus in the Protocol Exerciser for DigRF GUI.

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